Ecole de microélectronique et microsystèmes
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3D-IC Integration
Developments & Cooperations for servicing

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Agenda

- Introduction & Motivation for 3D-IC
- Process overview
- Partnership for MPW runs service
- 3D-IC Design Platform
- Conclusion

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure“ IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

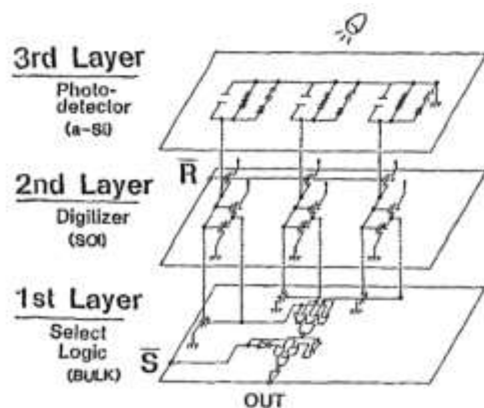

Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

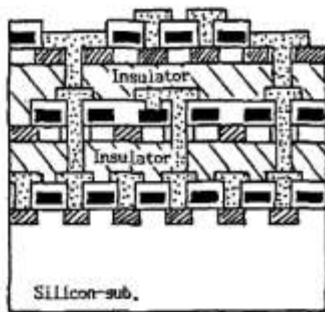

Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

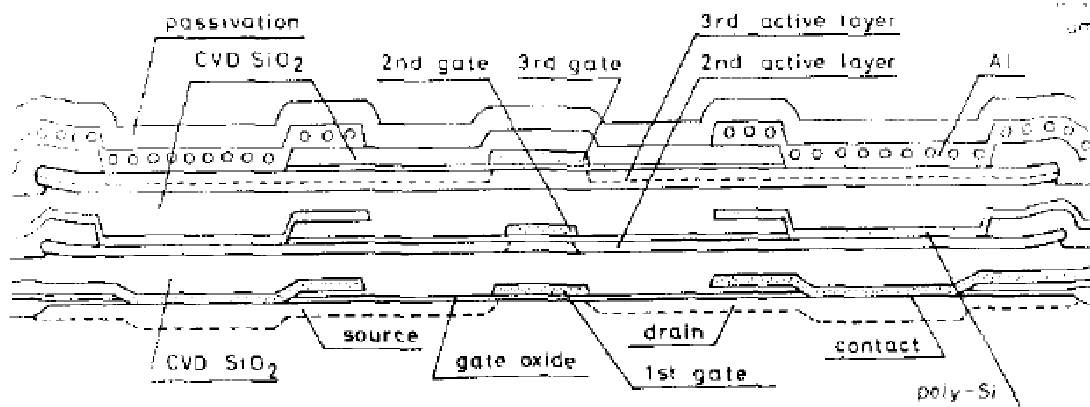

Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

3D-IC Integration : The Other Path for Scaling

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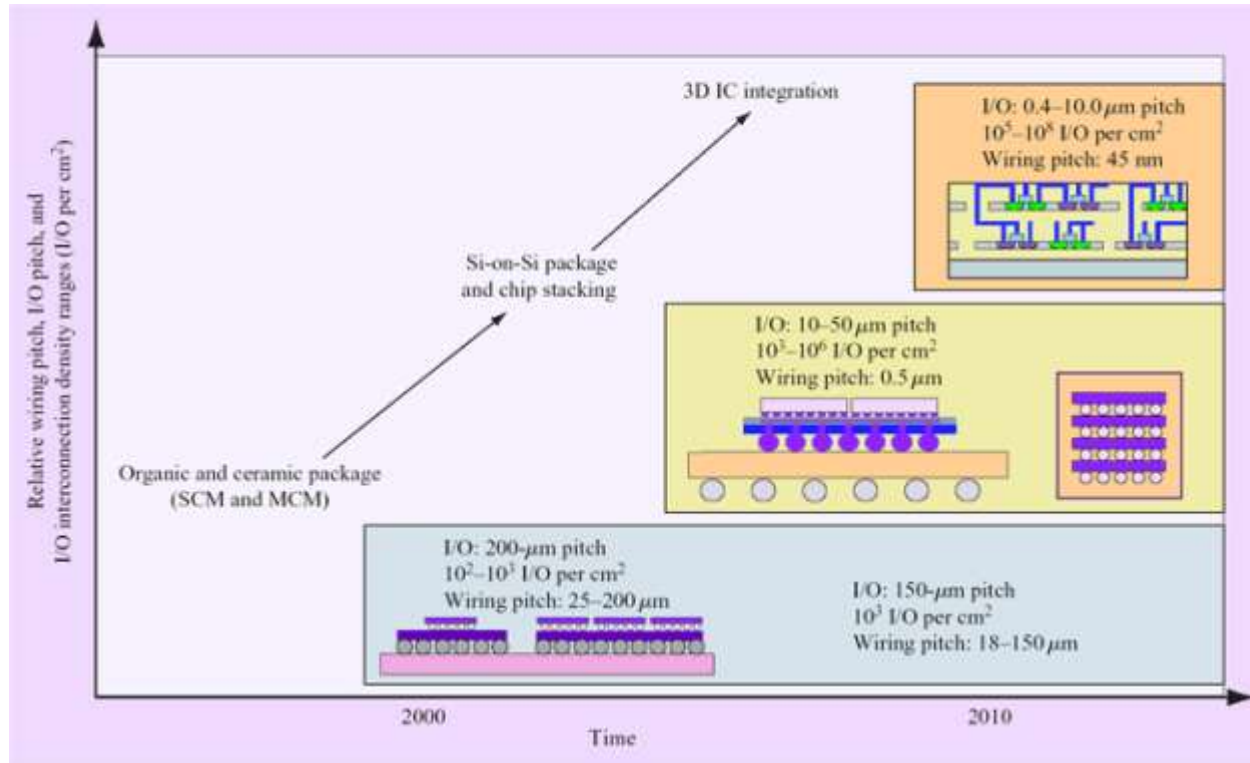


Source IBM http://www.research.ibm.com/journal/rd/526/knickerbocker.html

- **Moore's law by scaling conventional CMOS involves huge investments.**

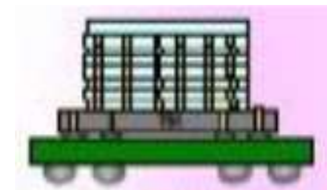
- **3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.**

- **Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at "reasonable" costs.**

Two Worlds with Different Integration Approaches

"Monolithic"

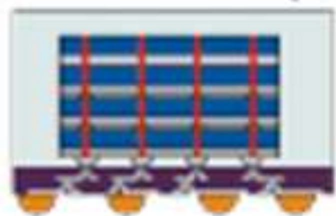
Distributing a whole system across several tiers



Heterogeneous Multi layer 3D-IC TSV integrated

3D-IC TSV integrated

3D-IC face to face

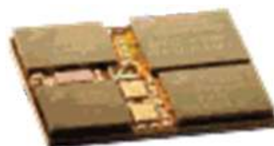


3D-IC TSV Stacked Memory

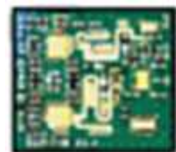
Integration

Silicon Interposer to high Integrated MCM

Die to Die Integrated package



Multi-Chip Module



Substrate based Module (PCB)

"Discrete"

Assembly of "Known Good Dies"

Which Design Methodology ?

- Discrete : 3D packaging, stacked dies, …

  1- Design a whole system.
  2- Split it in subsystems.
  3- Place the subsystems as predefined "Known Good Dies" (IPs).
  4- Determine and place the interfaces in between.
  5- The system is done

- Monolithic : 3D-IC Integration

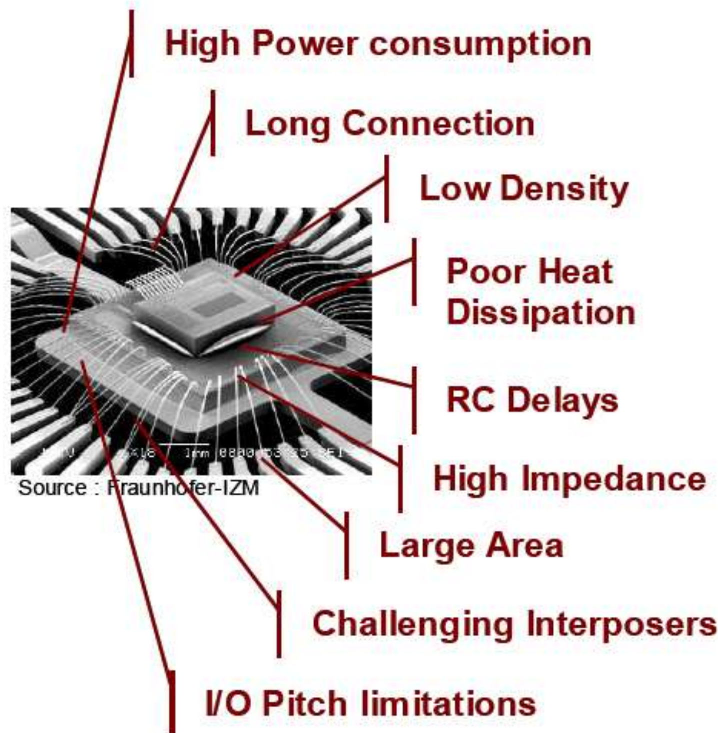
  1- Design a whole system.
  2- Split it in subsystems.
  3- Determine and place the interfaces in between.
  4- Generate and Place the subsystems in between the interfaces.
  5- The system is done

Here comes the difference : The "key" for a true 3D-IC Integration

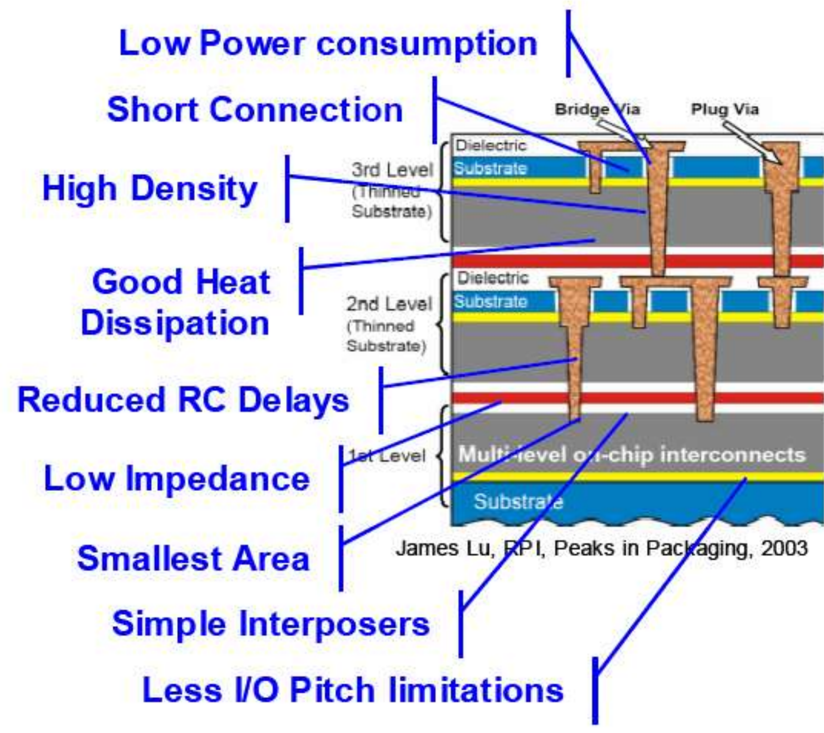
SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



Source : Fraunhofer-IZM



James Lu, RPI, Peaks in Packaging, 2003

TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

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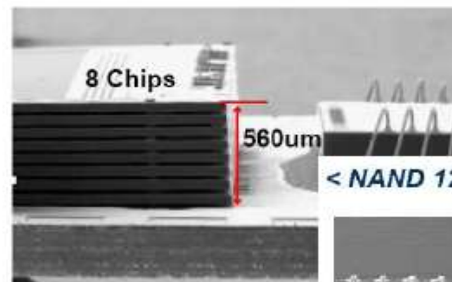
3D-IC Applications

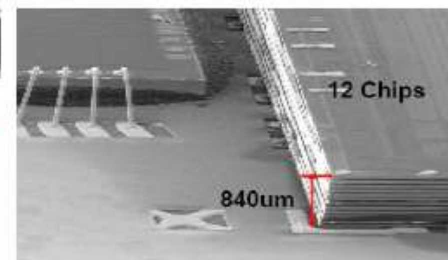
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

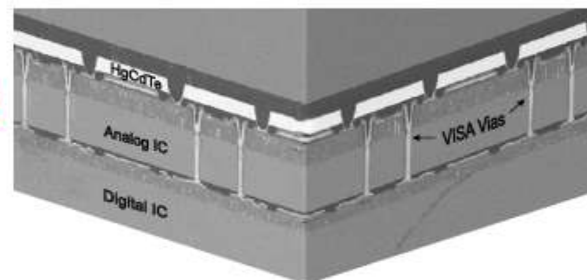


< NAND 12 Stacked Memory Card >



Samsung - 30 um laser drilled vias in 70um chips

RTI Infrared Imager

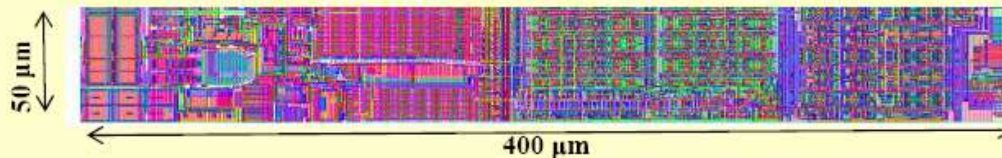


LHC-ILC Workshop on 3D Integration Techniques

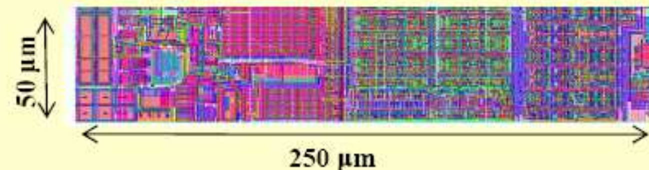
3D Microelectronics for Physics (FermiLab, IN2P3, INFN, CERN)

Expected feedback from 3D for SLHC

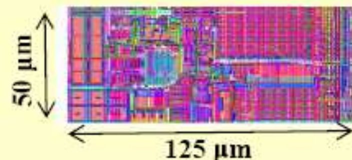
ATLAS Pixel Front End size



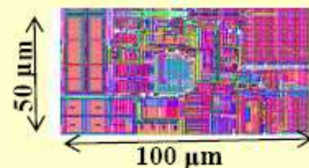
FE-I3 CMOS 250 nm

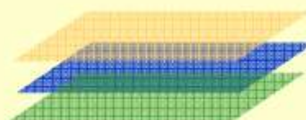


FE-I4 CMOS 130 nm



FE-I4-3D-2 CMOS 130 nm 2 layers

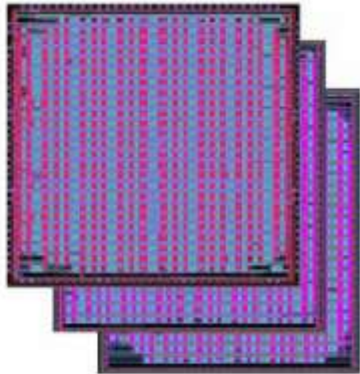




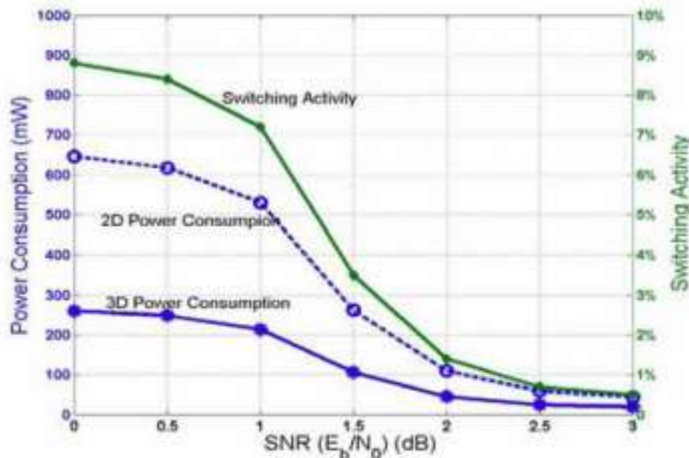
FE-I4-3D-3 CMOS 130 nm 3 layers

3D LHC 29 November 2007 A.Rozanov 5

Large Systems Benefits from 3D-IC Integration


Final layout view of 3D LDPC structure.

"Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"
Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi
University of Washington
International Conference on Computer Design, ICCD, Oct. 2007



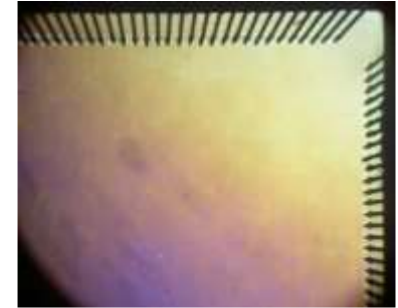
Post-layout power of the LDPC decoder (2D vs 3D).

Comparison between 3D and 2D designs

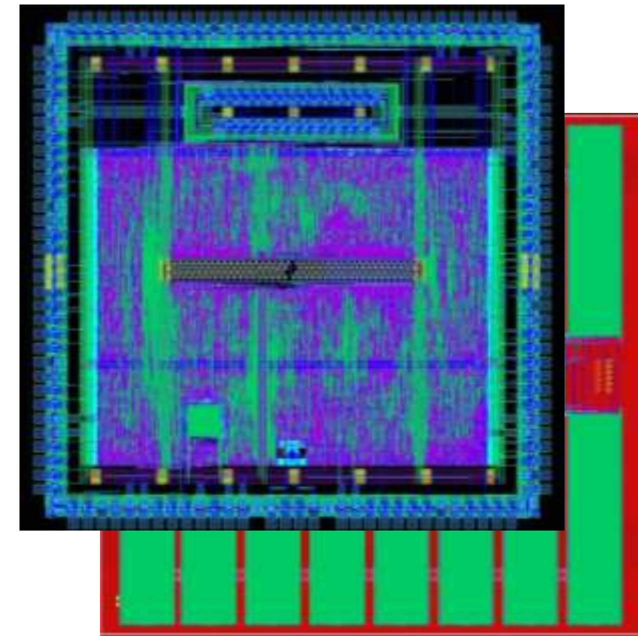
	2D design	3D design
Area (mm*mm)	18.238*15.92 =**290.35**	(6.4*6.227)*3 = **119.56**
Total wire length (m)	**182.42**	22.39+22.57+22.46 =**67.42**
Max WL before buffer insertion (mm)	**13.82**	**8.68**
Max WL after buffer insertion (mm)	**4**	**4**
Buffer used	**32900**	**24636**
Clock skew (ns)	**2.33**	**1**
Power dissipation (mw)	**646.2**	**260.2**

Performance Factor (Area * Timing * Power) = 14

An Illustration: CPU/Memory Stack



- R8051 CPU
  - 80MHz operation; 140MHz Lab test (VDD High)
  - 220MHz Memory interface
- IEEE 754 Floating point coprocessor
- 32 bit Integer coprocessor
- 2 UARTs, Int. Cont., 3 Timers, …
- Crypto functions
- 128KBytes/layer main memory



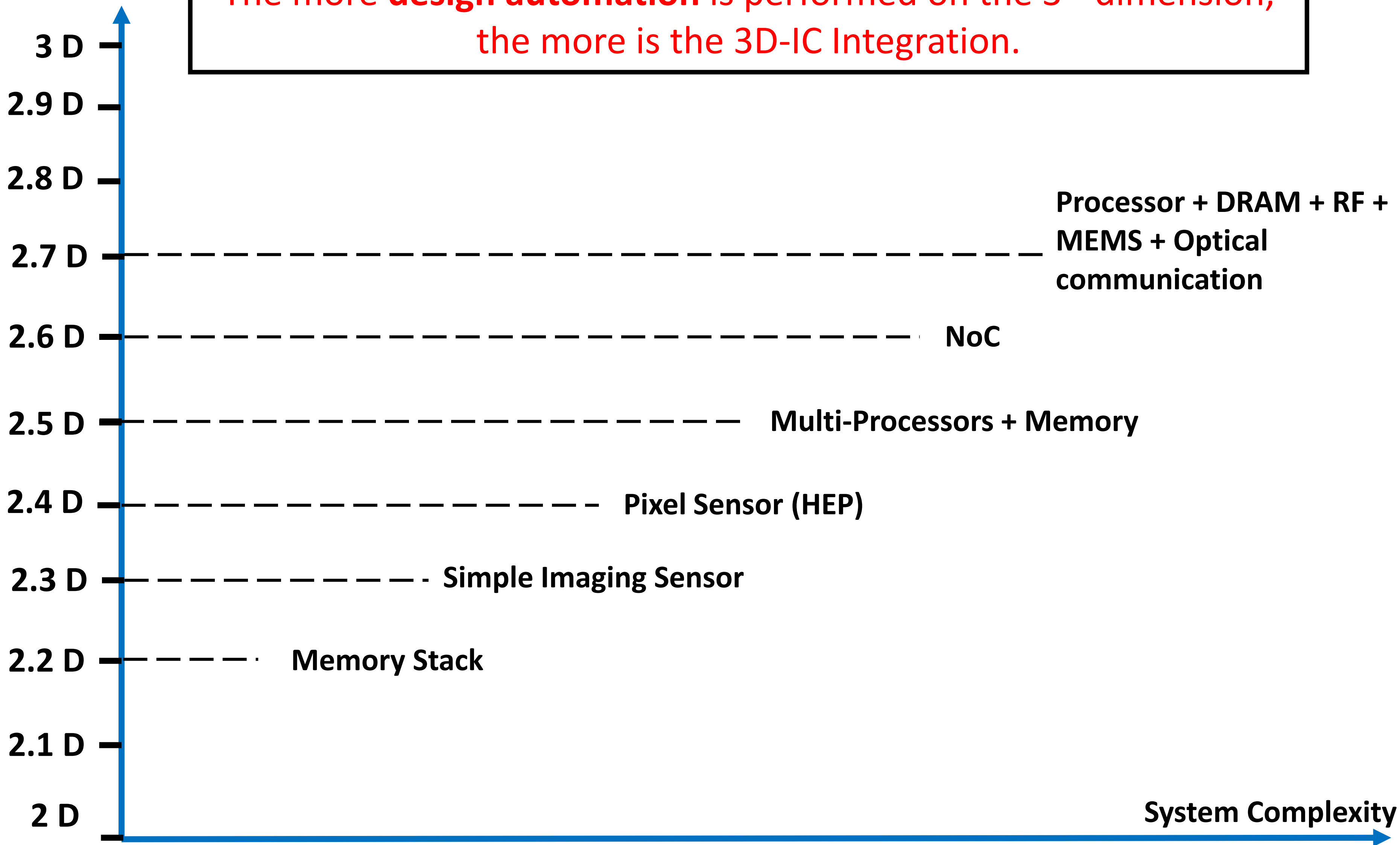
- 5X performance
- 1/10th Power

Source Tezzaron (2004)

Some 3D-IC Applications

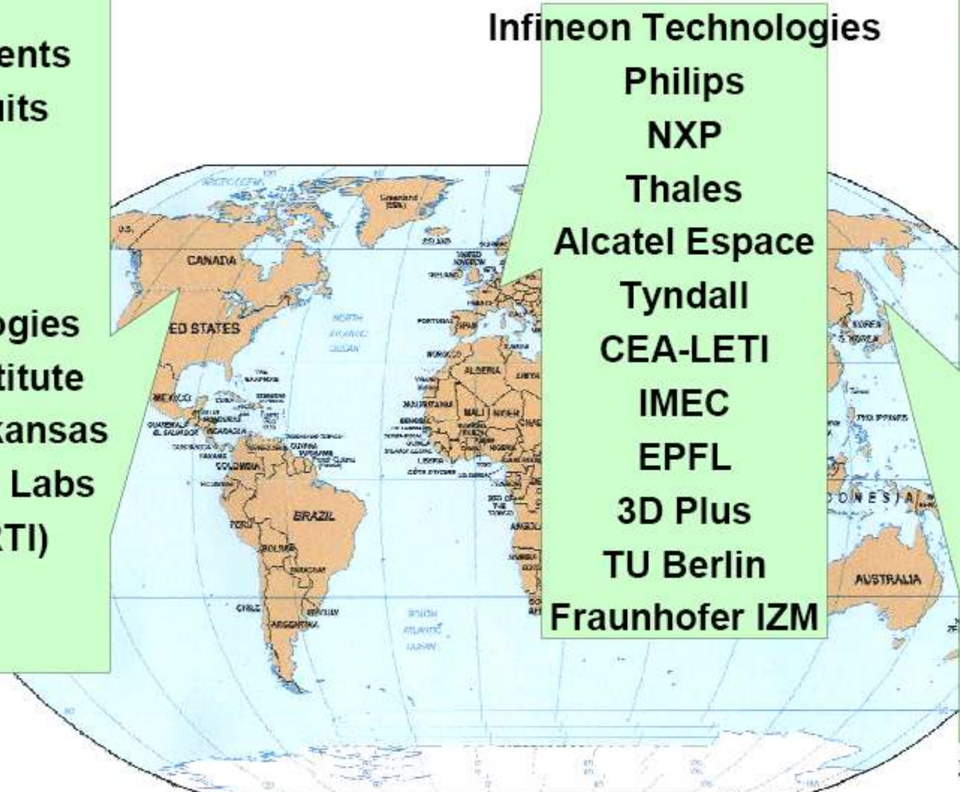
- **Pixel array for Particle detection (HEP community)**
  (Pixel sensor + Analog + Digital + Memory + high speed I/Os)
- **CMOS Image Sensor (Sensor + Processor + Memory)**
- **3D stacked Memories (Flash, DRAM, etc…)**
- **Multi-cores Processor + Cache Memory**
- **NoC (Network on Chip)**
- **Processor + DRAM + RF + MEMS + Optical communication + …**

Design Methodology



CMC-CMP-MOSIS Collaboration

Global Activities in 3D Integration



Irvine Sensors
IBM
Intel
Texas Instruments
Vertical Circuits
Amkor
Tessera
Tezzaron
Tru-Si Technologies
Rensselaer Institute
University of Arkansas
Sandia National Labs
MCNC-RDI (RTI)
MIT
Ziptronix

Infineon Technologies
Philips
NXP
Thales
Alcatel Espace
Tyndall
CEA-LETI
IMEC
EPFL
3D Plus
TU Berlin
Fraunhofer IZM

ASET
NEC
Tohoku University
University of Tokyo
ZyCube
CREST
Fujitsu
Sanyo
Sony
Toshiba
Denso
Mitsubishi
Sharp
Hitachi
Matsushita
Samsung

EMC 3D

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

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CMC / CMP / MOSIS partnering for 3D-IC process access

- **Stimulate the activity by sharing the expenses for manufacturing.**

- **Join forces for the technical support, and dedicate the roles for each partner.**

- **Make easier the tech support for local users respectively by each local center.**

- **Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.**

CMC-CMP-MOSIS partnering on 3D-IC

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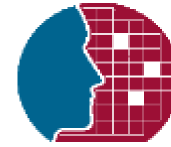


CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is scheduled to 31 May 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : **cmp@imag.fr**

CNRS – INPG – UJF

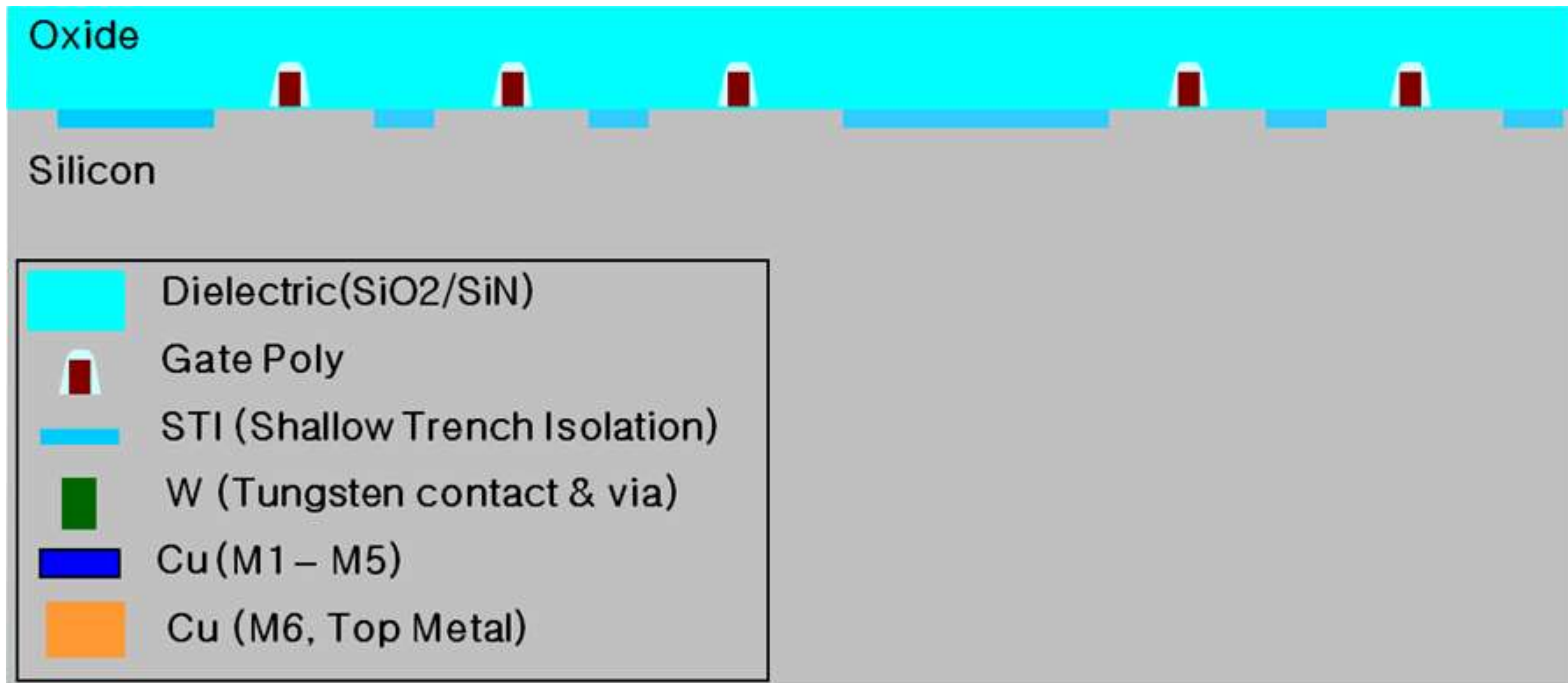
CMC - CMP - MOSIS Cooperation

- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers

Tezzaron 2-Tier Process (130nm CMOS)

Process Overview

Tezzaron Process Flow for TSV and DBI (using Via Middle process)

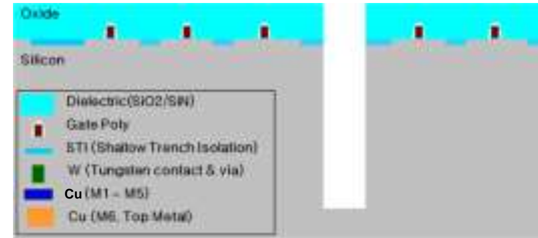


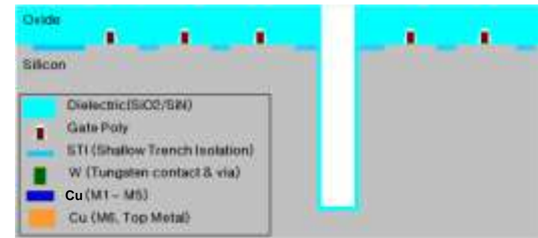
Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as DBI)

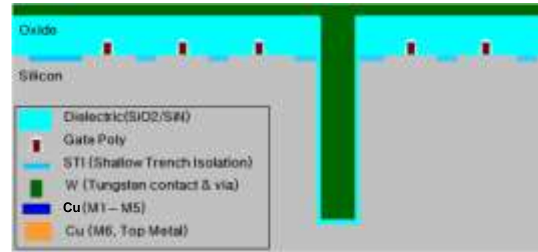
Source Tezzaron

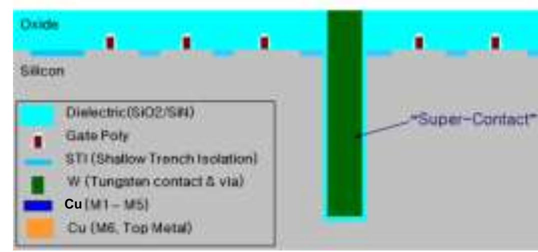
Tezzaron Process Flow for TSV and DBI (using Via Middle process)

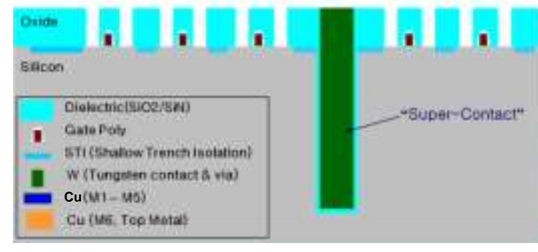
CNRS – INPG – UJF

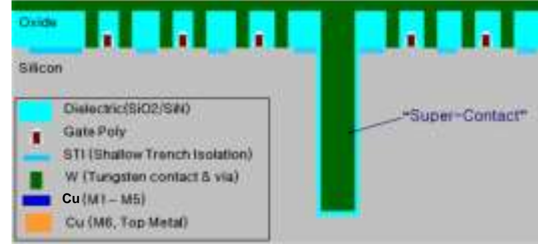


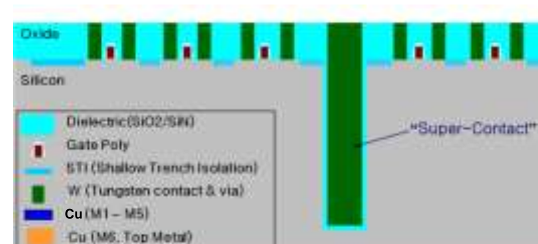


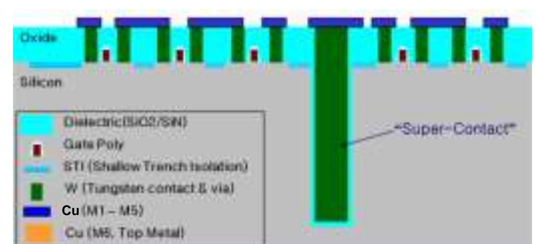


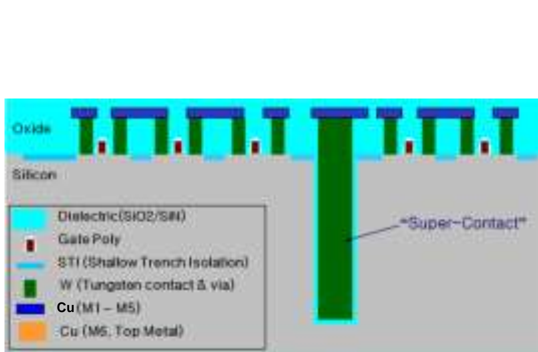


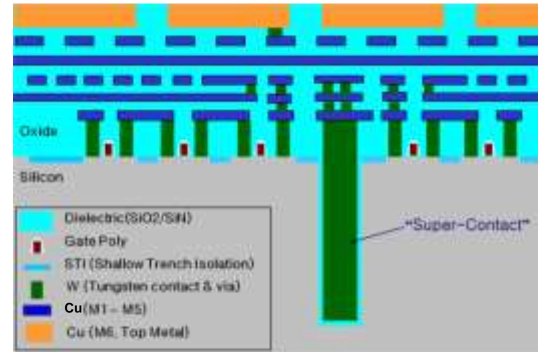




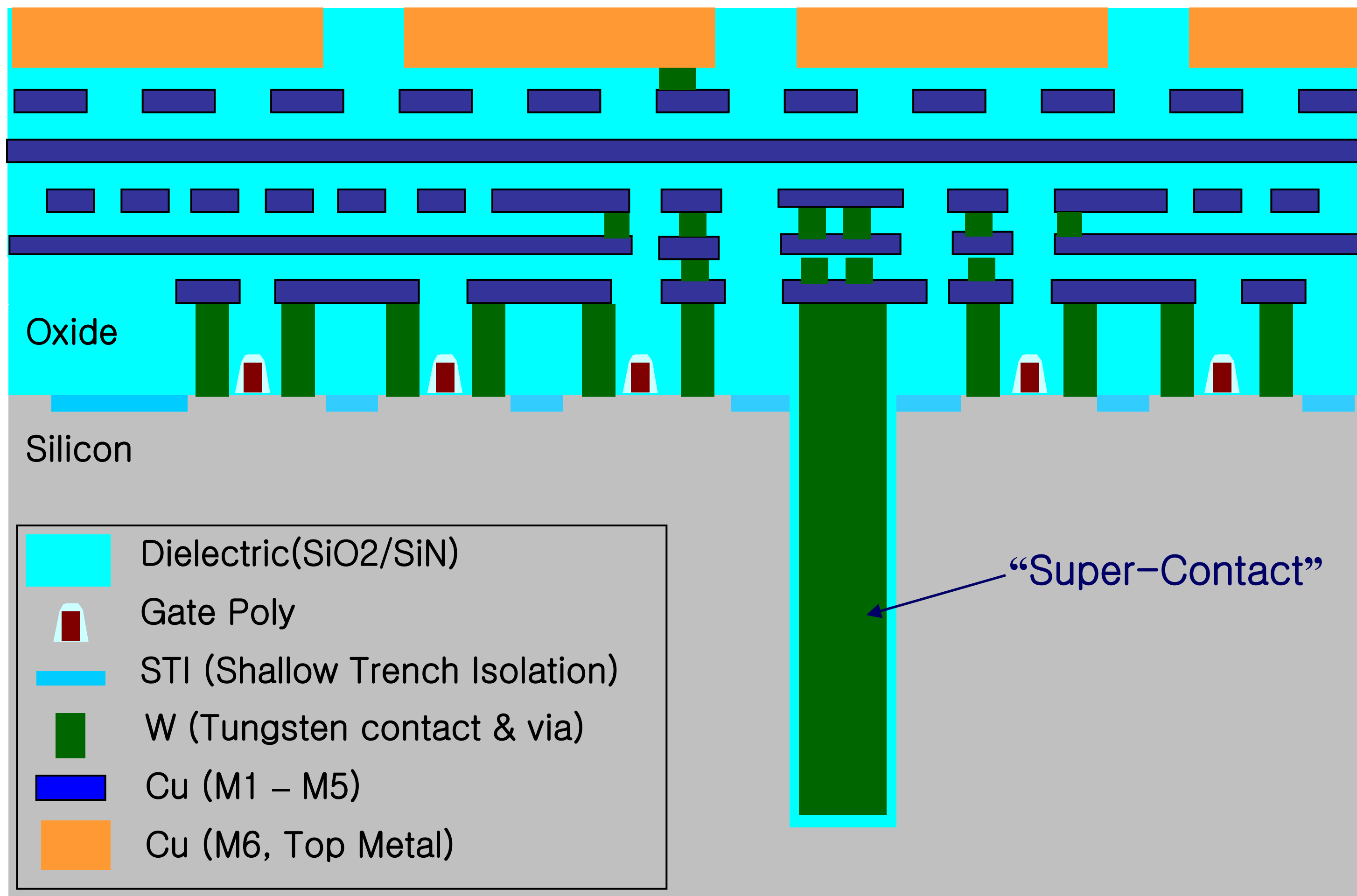






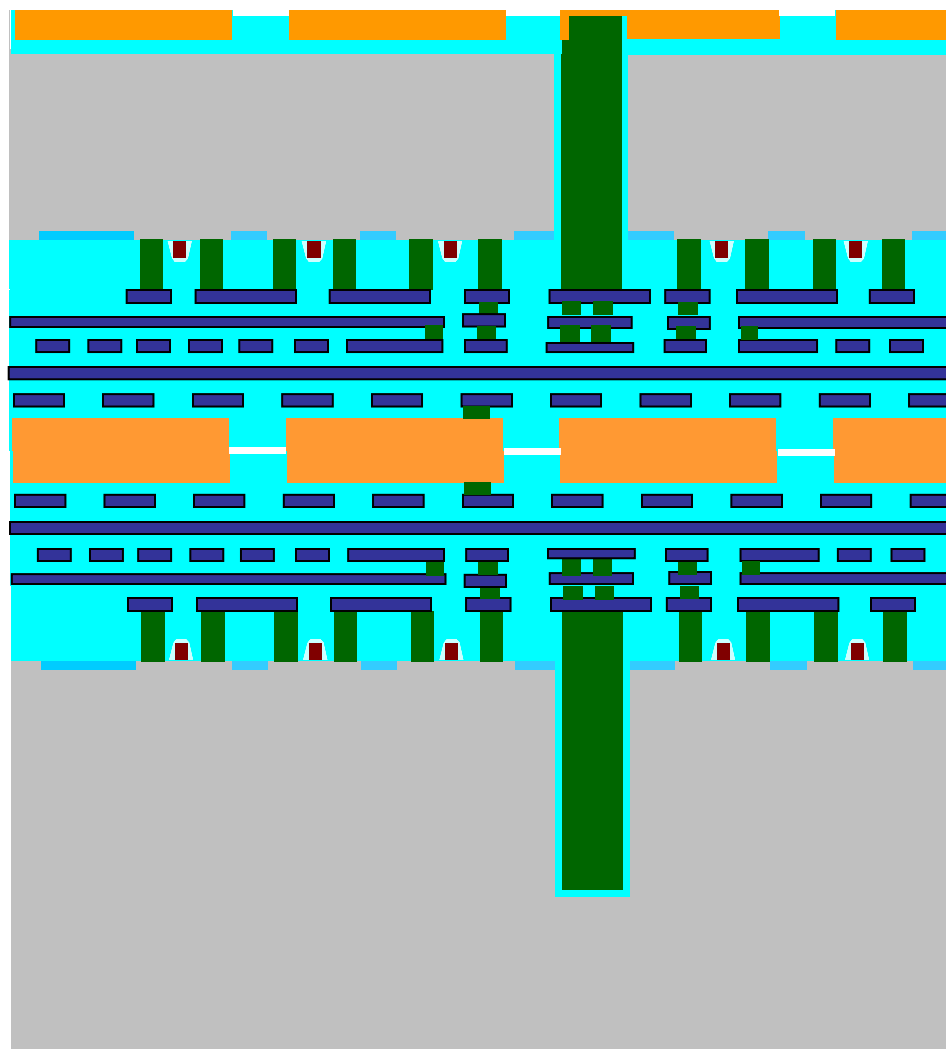


A Closer Look at Wafer-Level Stacking



Source Tezzaron

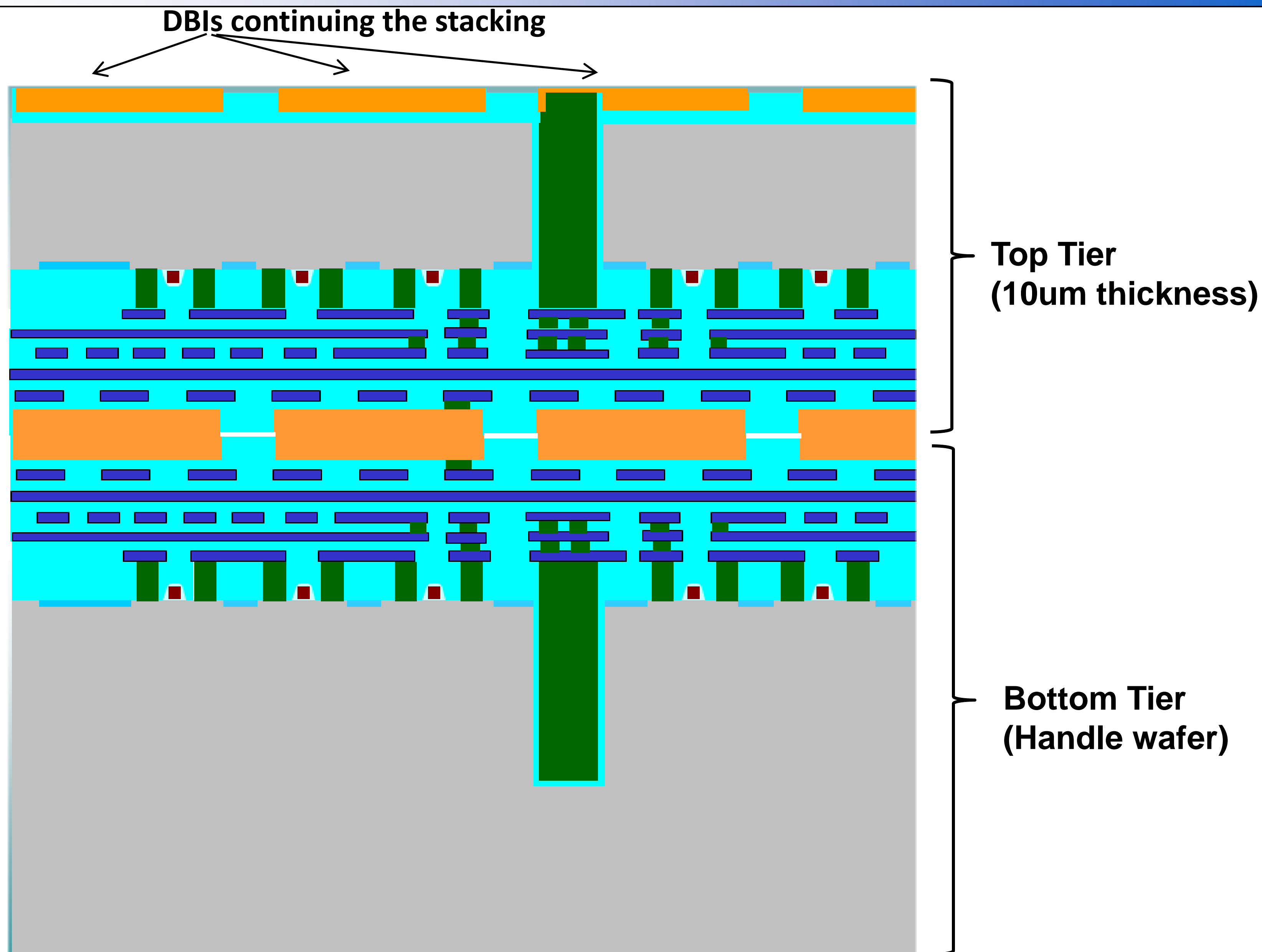
Next, Stack a Second Wafer & Thin:



Source Tezzaron

CNRS – INPG – UJF

Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)



Source Tezzaron

Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)

Bond pad for wire bonding or bump, flip-chip ...

Top Tier
(10um thickness)

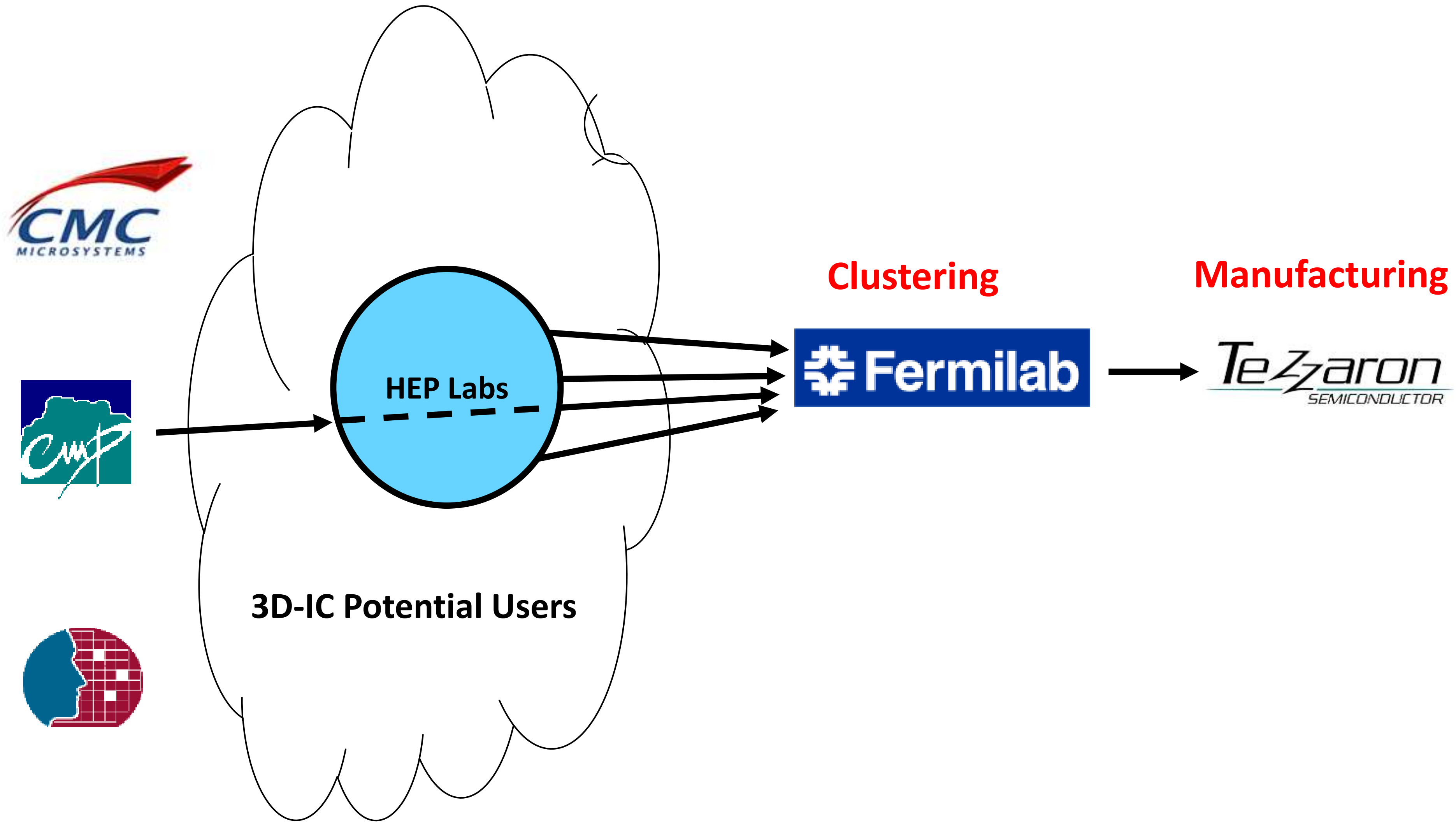
Bottom Tier
(Handle wafer)

Source Tezzaron

3D-IC MPW runs

3D-IC MPW Initial Infrastructure

First MPW Run organized by FermiLab using an Industrial Process

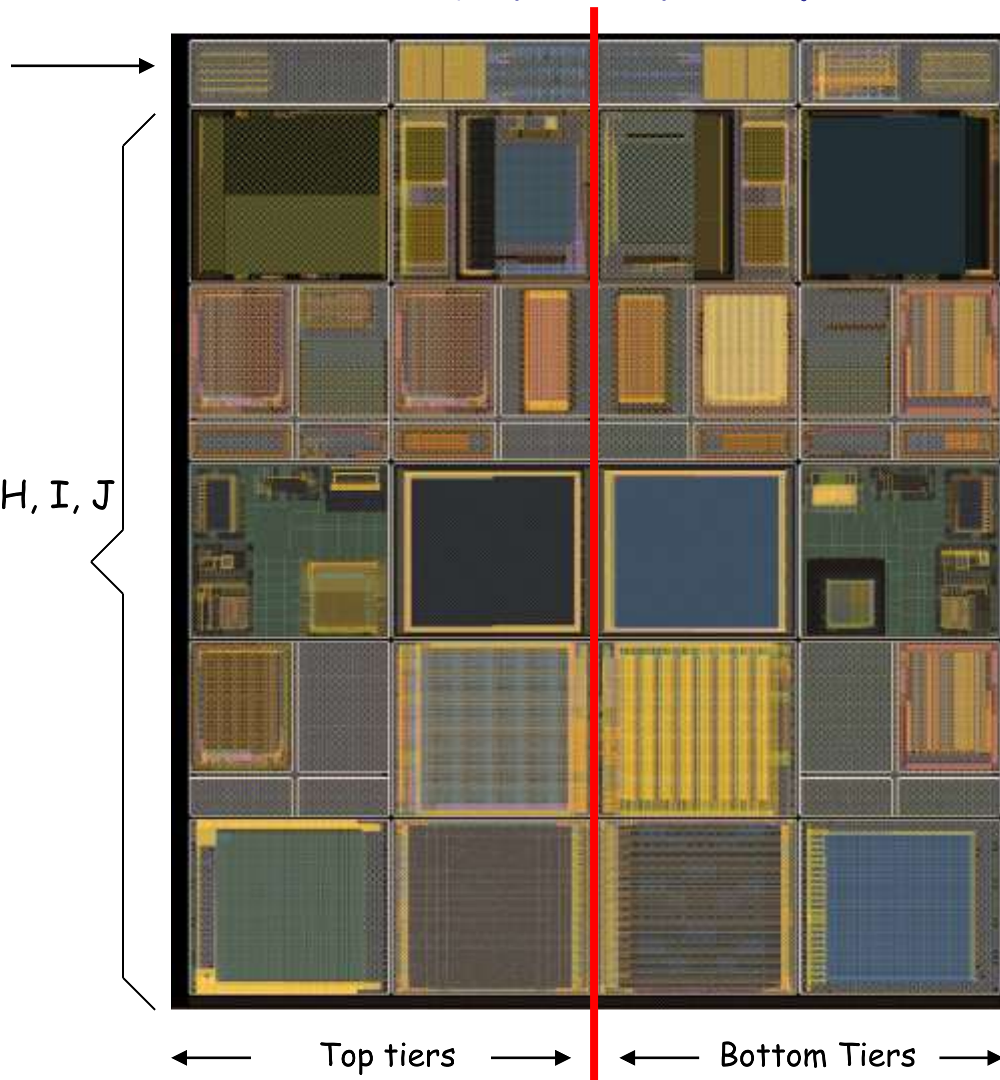


3D Consortium : 1st MPW run

MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D, E, F, G, H, I, J
5.5 x 6.3 mm



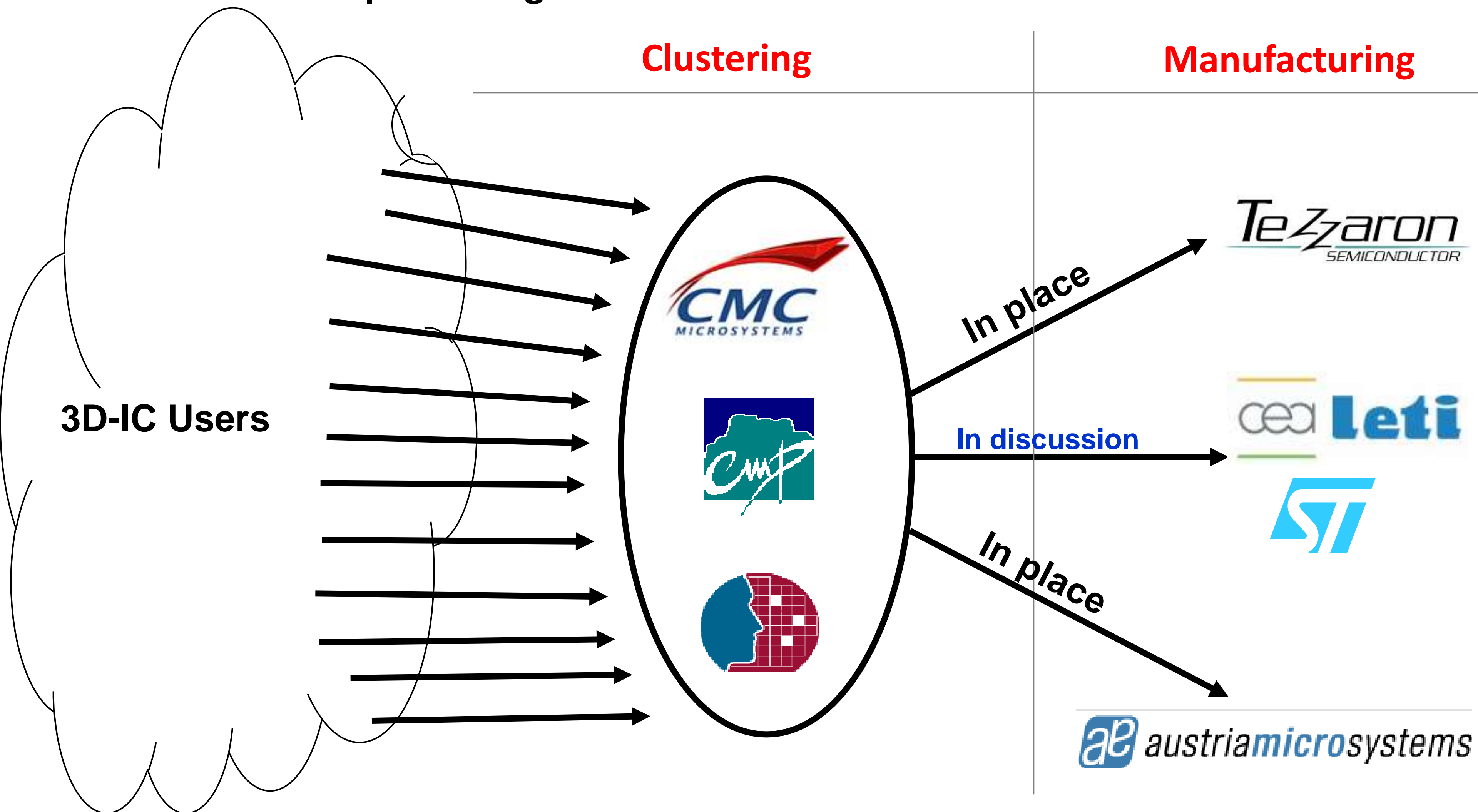
Top tiers | Bottom Tiers

Notice Symmetry about vertical center line

Source FermiLab (3D Consortium Meeting)

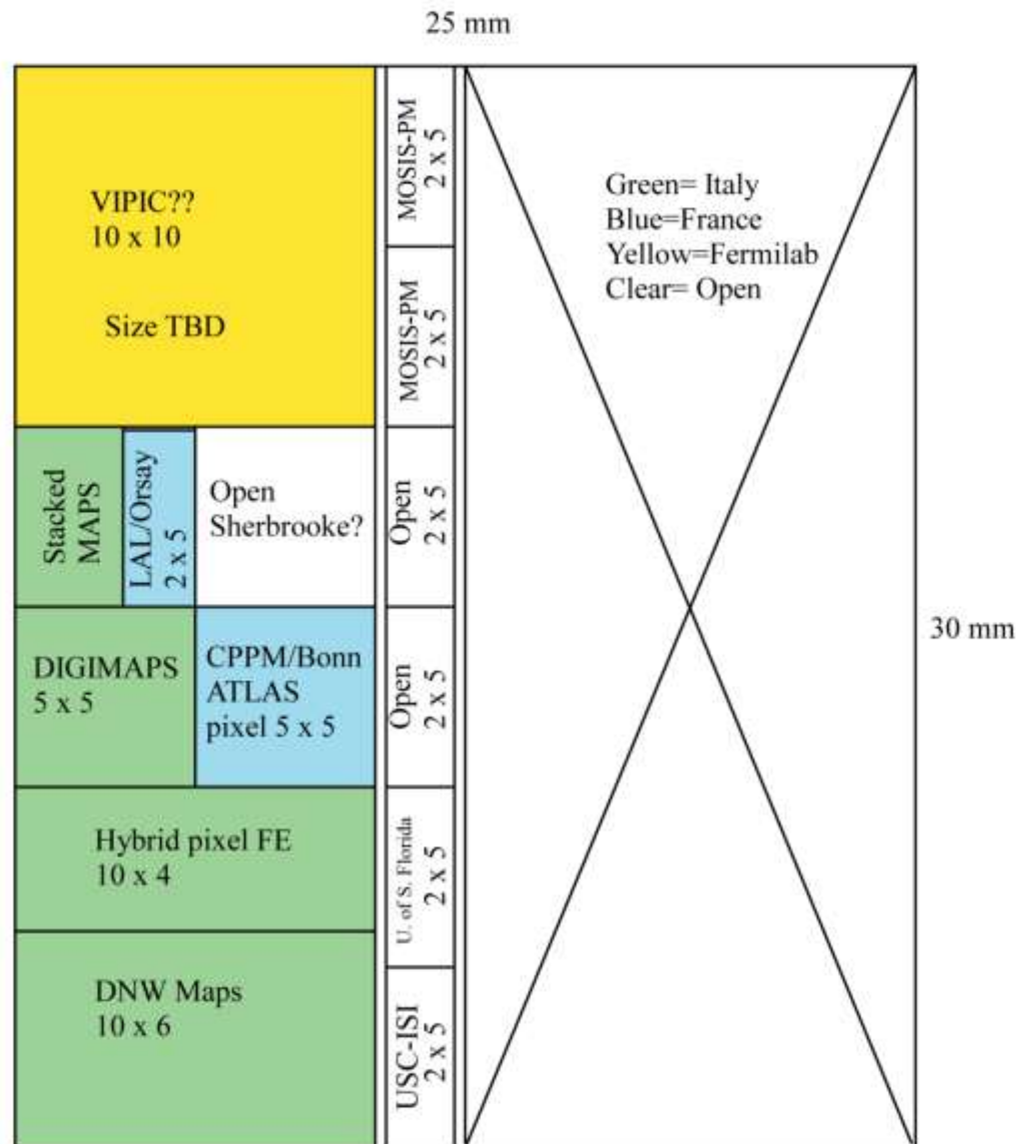
3D-IC MPW Infrastructure

CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Critical mass will allow frequent MPW runs and low pricing

CMP/MOSIS/CMC : 1st MPW run



MPW run deadline : May 31st, 2011

3D-IC Design Platform

Tezzaron / GlobalFoundries Design Platform

- The Design Platform is modular. It has all features for full-custom design or semi-custom automatic generation design.
  - **PDK :** ***Original PDK from GF + (TSV / DBI) definition***
  - **Libraries :** ***CORE and IO standard libraries from ARM***
  - **Memory compilers :** ***SPRAM, DPRAM and ROM from ARM***
  - **3D-IC Utilities :** ***Contributions developments embedded in the platform***
  - **Tutorials, User's setup.**
- All the modules inside the platform refer to a unique variable, making it portable to any site. The installation procedure is straightforward.
- Support of CDB and OpenAccess databases.

Tezzaron / GlobalFoundries Design Platform

Design documents included in the platform

BacksideBondPads1_1.pdf	Tezzaron Backside Bond Pad Rules (rev. 1.1 / 4 June 2009)
Bond_Interface_Rules_1_0.pdf	Bond Interface Rules (rev. 1.0 / 18 July 2007)
MPW100109_Design_Guide_8.pdf	MPW100109 Design Guide (rev. 8 / 11 Feb. 2010)
SuperContact_Rules_2_11.pdf	SuperContact Rules (rev. 2.1 / 29 Jan 2008)
mpwMemSpec1_5.pdf	MPW100109 Memory specifications (rel. 1.5 / 16 Feb. 2010)
yi_108_dr001_1t.pdf	Release notes of the 130nm CMOS Design Rules Manual (version 1T)
yi_108_dr001_1t_oct2010.pdf	130nm CMOS Design Rules Manual (version 1T / Oct. 2010)
yi_108_ep004_1d.pdf	Release notes of the 130nm CMOS Electrical Parameters (version 1D)
yi_108_ep004_rev_1d.pdf	130nm CMOS Electrical Parameters (version 1D / 19 March 2010)

Black : GlobalFoundries Design Documents

Blue : Tezzaron Design Documents

Red : Tezzarom Design guide

PDK Tezzaron / GlobalFoundries

chrt13lprf_DK009_Rev_1D (Version issued in Q1 2011)

assura
calibre
cds_cdb
cds_oa
doc
eldo
hercules
hspice
prep3DLVS
skill
spectre
strmMaptables_ARM
strmMaptables_Encounter

assura:
FILLDRC
LVS
QRC

calibre:
3DDRC
3DLVS
DRC
FILLDRC
calibreSwitchDef

hercules:
DRC
LVS
STAR_RCXT

Collaborative Work to the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)

CNRS – INPG – UJF

Virtuoso Layout Editor with 3D layers and verification

Virtuoso from Cadence IC 5.1.41

TSV

Back Metal

Back Pad

DBI

Layer	Purpose
NO_FILL	drw
TSCSuperCnt	drw
TSCBackMet0	drw
TSCBackMet0	lbl
TSCBackMet1	drw
TSCBackMet1	lbl
TSCBPad	drw
SRAM_TSC	drw
PR_BNDRY	drw
NWELL	drw
DNWELL	drw
LDMOS_XTOR	mar
COMP	drw
POLY2	drw
POLY2	lbl
PPLUS	drw
NPLUS	drw
CNT	drw
MET1	drw
MET1	lbl
VIA1	drw
MET2	drw
MET2	lbl
VIA2	drw
MET3	drw
MET3	lbl
VIA3	drw
MET4	drw
MET4	lbl
VIA4	drw
MET5	drw
MET5	lbl
VIATOP	drw
METTOP	drw

X: 12.500 Y: -4.115 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 2

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Calibre Tezzaron Help

Calibre

Assura

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R:hiZoomAbsoluteScale(hiGetCurrentWi

>

Customized Menu with some utilities

CNRS – INPG – UJF

Virtuoso from Cadence IC 6.1.4

LSW

Sort Edit Help

NO_FILL drawing

Layer Object Grid

AV NV AS NS

NO_FILL drawing
TSCSuperCnt drawing
TSCBackMet0 drawing
TSCBackMet0 label
TSCBackMet1 drawing
TSCBackMet1 label
TSCBPad drawing
SRAM_TSC drawing
PR_BNDRY drawing
NWELL drawing
DNWELL drawing
LDMOS_XTOR marking
COMP drawing
POLY2 drawing
POLY2 label
PPLUS drawing
NPLUS drawing
CNT drawing
MET1 drawing
MET1 label
VIA1 drawing
MET2 drawing
MET2 label
VIA2 drawing
MET3 drawing
MET3 label
VIA3 drawing
MET4 drawing
MET4 label
VIA4 drawing
MET5 drawing
MET5 label
VIATOP drawing
METTOP drawing
METTOP label
RDL_MK marking
LPN_dg drawing

Virtuoso® Layout Suite L Reading: CORELIB_LP allcells_CORELIB_LP layout

Launch File Edit View Create Verify Connectivity Options Tools Window Assura Calibre Help cadence

*New Layers Colors
*GF Layers Colors
*myLSW
*pgText
*ZoomXY
About Tezzaron

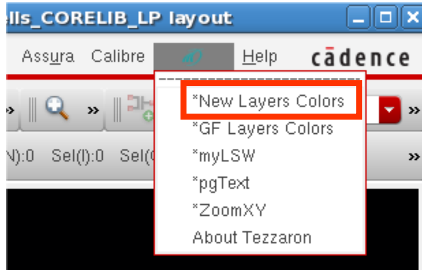
(F)Select:0 Sel(N):0 Sel(I):0

mouse L: mouseSingleSelectPt() M: hiRedraw() R: _lxHiMousePopUp()

2(3) > Cmd:

Utility to change automatically from GF colors to new colors

CNRS – INPG – UJF



LSW

Sort Edit Help

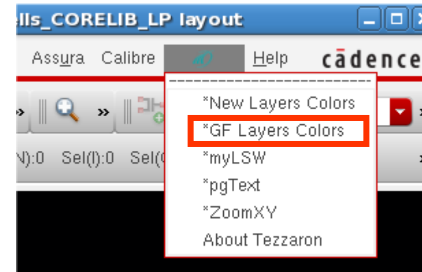
NO_FILL drawing

chrt013lp

Layer | Object | Grid

AV NV AS NS

Layer	Purpose
NO_FILL	drawing
TSCSuperCnt	drawing
TSCBackMet0	drawing
TSCBackMet0	label
TSCBackMet1	drawing
TSCBackMet1	label
TSCBPad	drawing
SRAM_TSC	drawing
PR_BNDRY	drawing
NWELL	drawing
DNWELL	drawing
LDMOS_XTOR	marking
COMP	drawing
POLY2	drawing
POLY2	label
PPLUS	drawing
NPLUS	drawing
CNT	drawing
MET1	drawing
MET1	label
VIA1	drawing
MET2	drawing
MET2	label
VIA2	drawing
MET3	drawing
MET3	label
VIA3	drawing
MET4	drawing
MET4	label
VIA4	drawing
MET5	drawing
MET5	label
VIATOP	drawing
METTOP	drawing
METTOP	label
RDL_MK	marking
LPN_dg	drawing



LSW

Sort Edit Help

NO_FILL drawing

chrt013lp

Layer | Object | Grid

AV NV AS NS

Layer	Purpose
NO_FILL	drawing
TSCSuperCnt	drawing
TSCBackMet0	drawing
TSCBackMet0	label
TSCBackMet1	drawing
TSCBackMet1	label
TSCBPad	drawing
SRAM_TSC	drawing
PR_BNDRY	drawing
NWELL	drawing
DNWELL	drawing
LDMOS_XTOR	marking
COMP	drawing
POLY2	drawing
POLY2	label
PPLUS	drawing
NPLUS	drawing
CNT	drawing
MET1	drawing
MET1	label
VIA1	drawing
MET2	drawing
MET2	label
VIA2	drawing
MET3	drawing
MET3	label
VIA3	drawing
MET4	drawing
MET4	label
VIA4	drawing
MET5	drawing
MET5	label
VIATOP	drawing
METTOP	drawing
METTOP	label
RDL_MK	marking
LPN_dg	drawing

Libraries from Providers and Users

Library Manager: WorkArea: /cmp/kit_F/TDP_2011q2v1_oa

File Edit View Design Manager Help — cādence

Show Categories | Show Files

Library: CORELIB_LP

- 3DICLIB
- 3D_Frames ← Univ. Bonn
- 3dCheck ← NCSU
- 3dexample
- CORELIB_LP } ARM
- CORELIB_LP_LVT } ARM
- IOLIB_IL } ARM
- IOLIB_STRGD } ARM
- PadringLib ← IPHC
- US_8ths
- ahdlLib
- analogLib
- avTech
- basic
- cdsDefTechLib
- charteredFermiLibrary ← FermiLab
- chrt013lp } GF/TSC
- chrt013rf } GF/TSC
- functional
- rfExamples
- rfLib

Category: AND

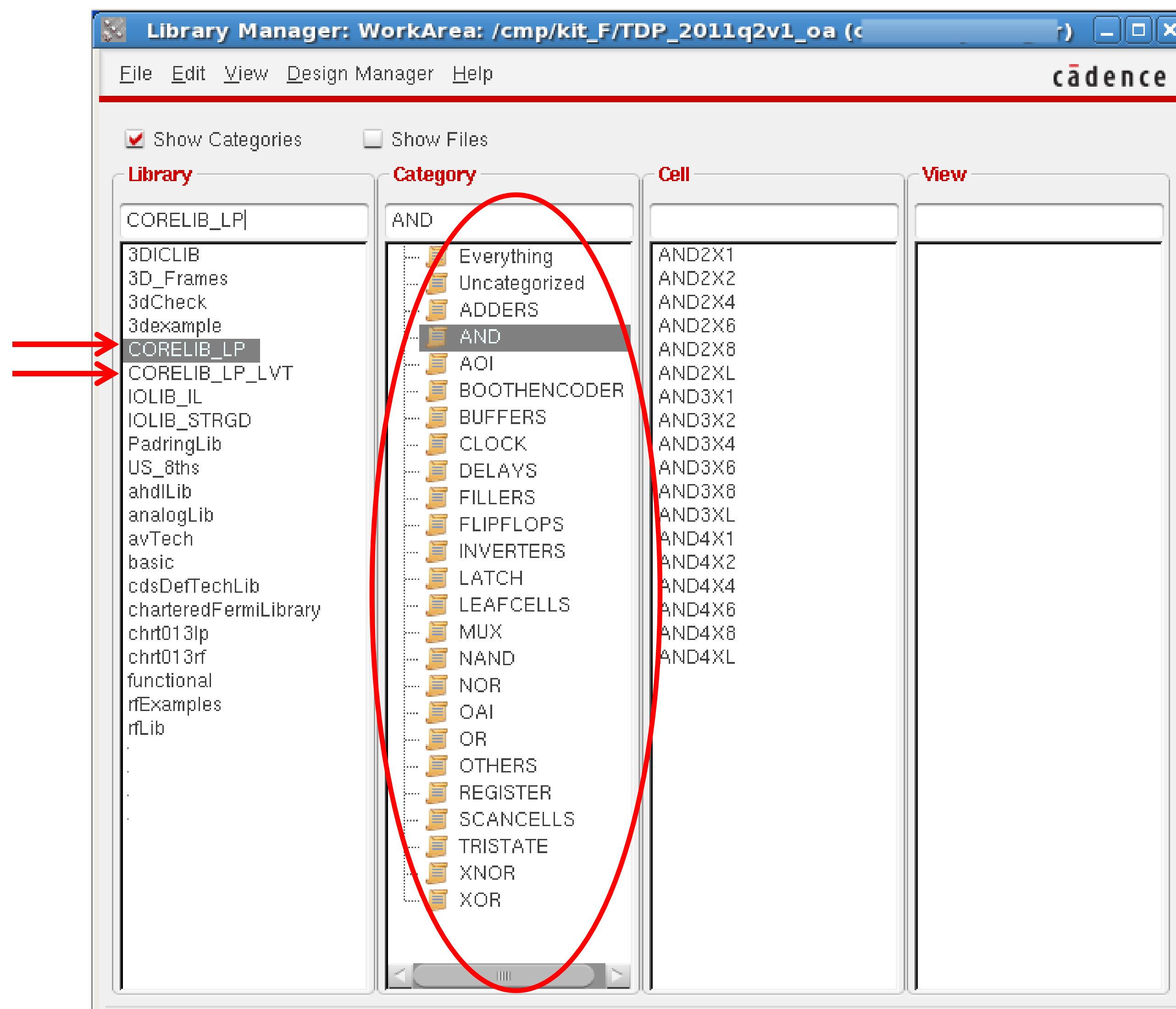
- Everything
- Uncategorized
- ADDERS
- AND
- AOI
- BOOTHENCODER
- BUFFERS
- CLOCK
- DELAYS
- FILLERS
- FLIPFLOPS
- INVERTERS
- LATCH
- LEAFCELLS
- MUX
- NAND
- NOR
- OAI
- OR
- OTHERS
- REGISTER
- SCANCELLS
- TRISTATE
- XNOR
- XOR

Cell

- AND2X1
- AND2X2
- AND2X4
- AND2X6
- AND2X8
- AND2XL
- AND3X1
- AND3X2
- AND3X4
- AND3X6
- AND3X8
- AND3XL
- AND4X1
- AND4X2
- AND4X4
- AND4X6
- AND4X8
- AND4XL

View

ARM / Artisan Digital CORE Libraries



ARM / Artisan Digital & Analog IO Libraries

CNRS – INPG – UJF

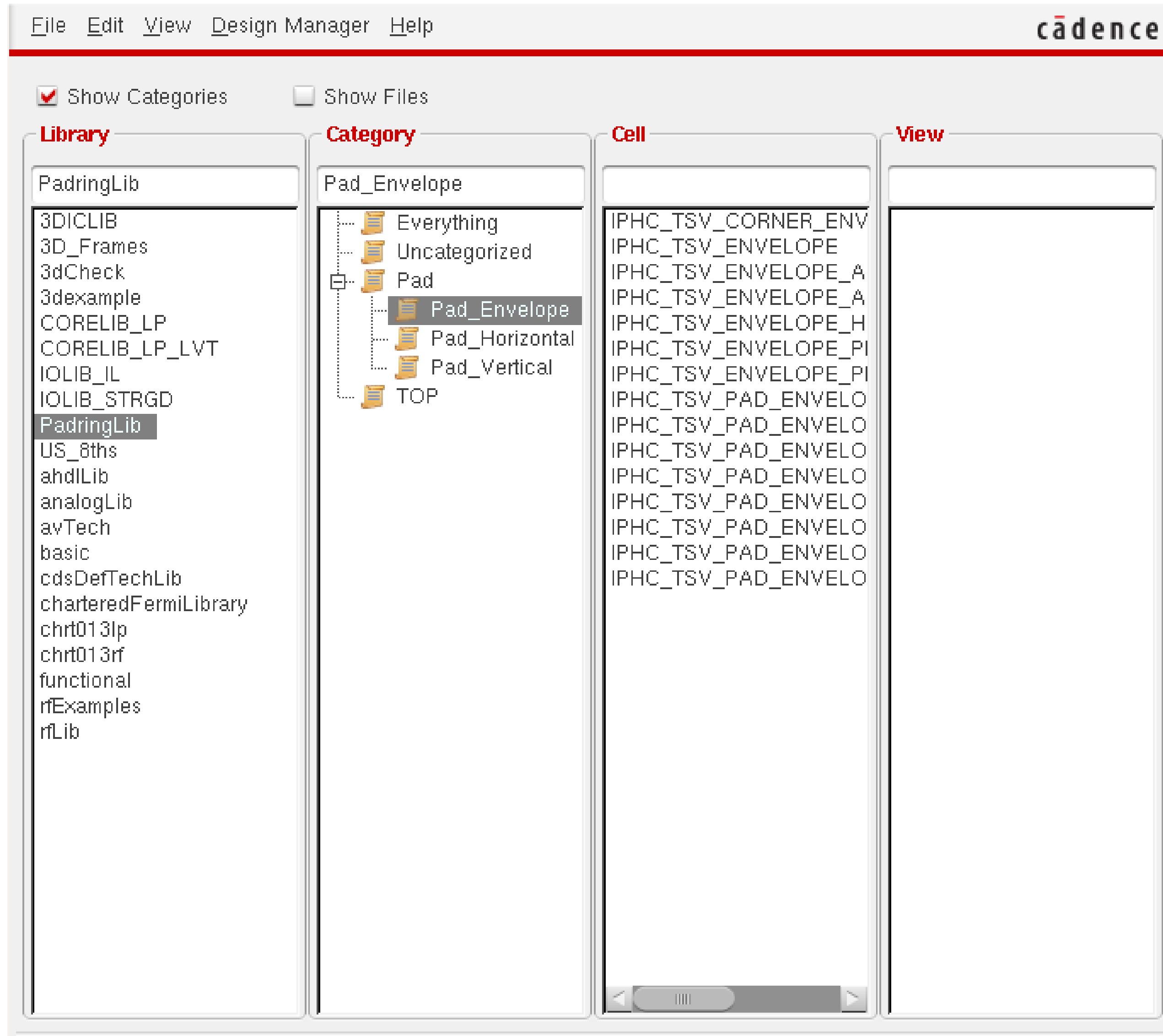
File Edit View Design Manager Help
cādence

Show Categories
Show Files

Library	Category	Cell	View
IOLIB_IL	Uncategorized		
3DICLIB	Everything		
3D_Frames	Uncategorized		
3dCheck	FILLER_IOCELLS		
3dexample	IOCELLS		
CORELIB_LP	LEAF_CELLS		
CORELIB_LP_LVT	LEAF_IOCELLS		
IOLIB_IL	SUPPLIES		
IOLIB_STRGD			
PadringLib			
US_8ths			
ahdlLib			
analogLib			
avTech			
basic			
cdsDefTechLib			
charteredFermiLibrary			
chrt013lp			
chrt013rf			
functional			
rfExamples			
rfLib			

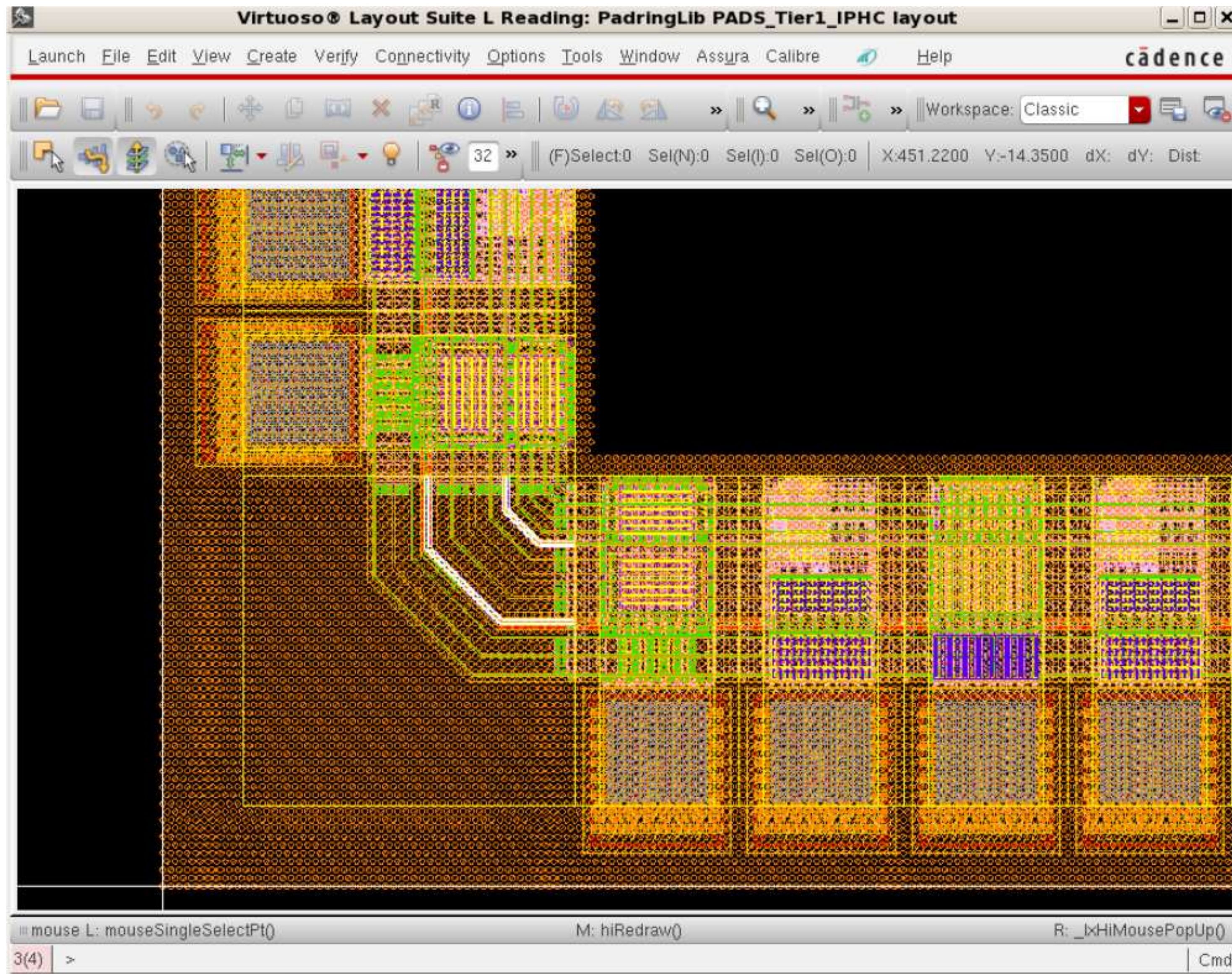
IPHC Contribution for 3D-IC IO Libraries

Pad shell (or envelop) containing TSV and DBI allowing using the ARM IO libraries in 3D-IC designs



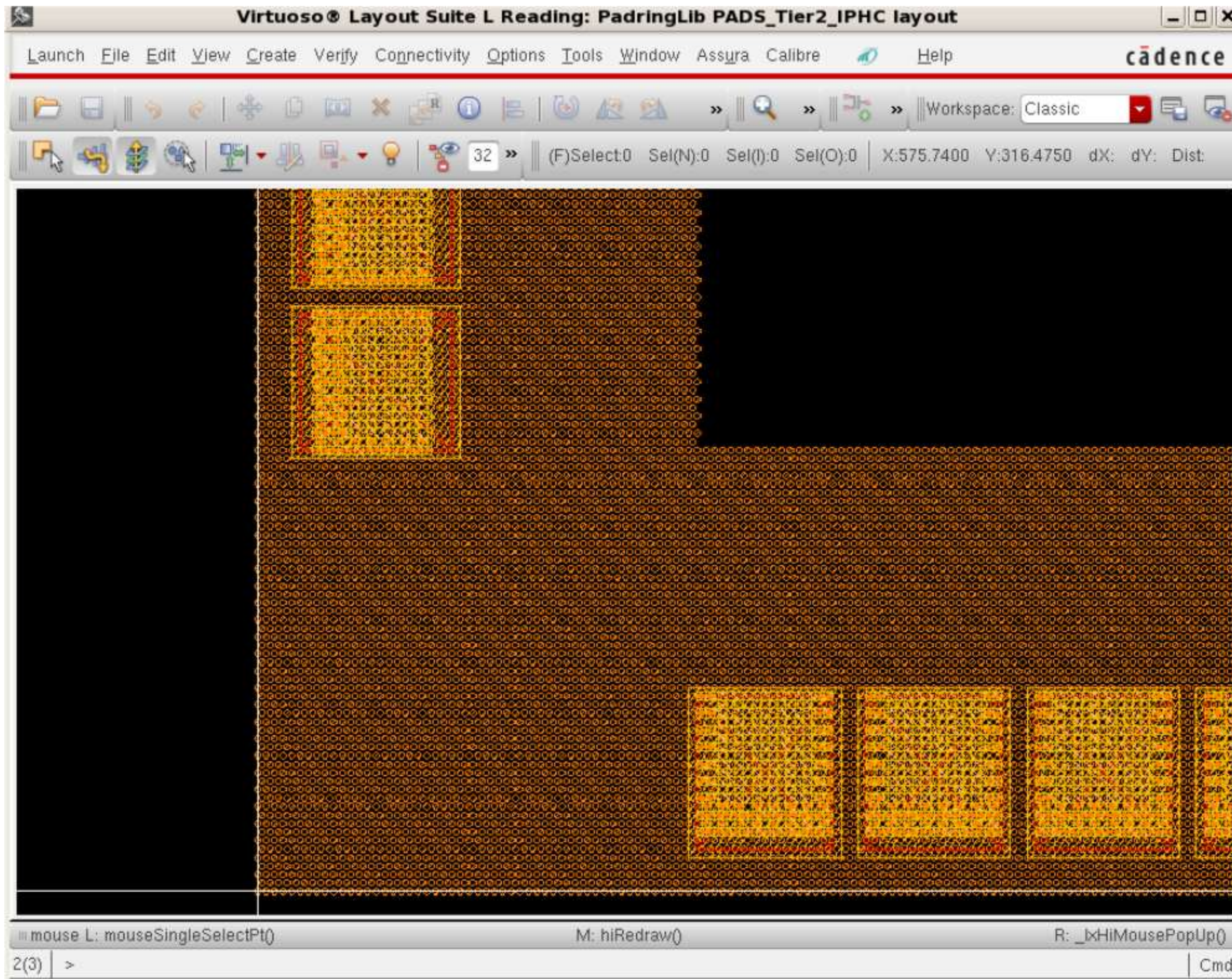
IPHC Contribution for 3D-IC IO Libraries

Pad shell (or envelop) containing TSV and DBI allowing using the ARM IO libraries in 3D-IC designs



IPHC Contribution for 3D-IC IO Libraries

Pad shell (or envelop) containing DBI and TSV connecting the pad to the backside bonding pad

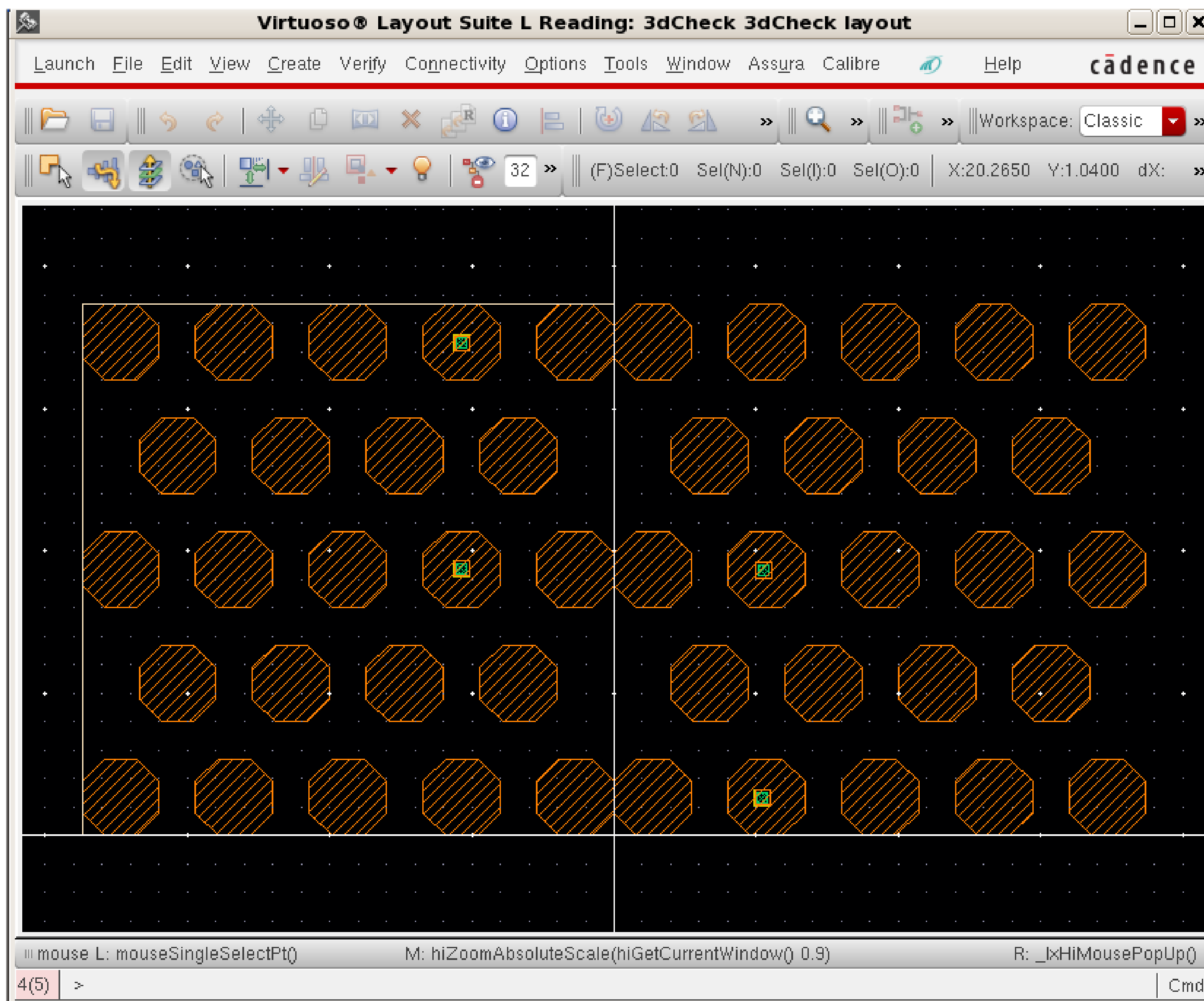


FermiLab Digital Library

Basic custom digital cells and IO pads

Virtuoso / Calibre 3D DRC Interactive Menu

CNRS – INPG – UJF



Virtuoso / Calibre DRC Interactive Menu

CNRS – INPG – UJF

Virtuoso® Layout Suite L Reading: test allcells_CORELIB_LP layout

Launch File Edit View Create Verify Connectivity Options Tools Window Assura Calibre Help cadence

Run DRC
Run DFM
Run LVS
Run PERC
Run PEX
Start RVE
Clear Highlights
Setup
About...

Setting switches graphically

Calibre Interactive - nmDRC

File Transcript Setup Help

Rules
Inputs
Outputs
Run Control
Transcript
Customization
Run DRC
Start RVE

DRC Rules File
$TDK_DIR/calibre/DRC/drc_header_1t_00
View Load

DRC Run Dire
drcRunDir

Layer Deriv

Customization Settings (calibreSwitchDef in /kit_F/TDP_2011

TEZZARON Switches For DRC Options

Checking Density rules is mandatory for sign-off DRC

Check Floating Bond Interface METTOP

OK Cancel Reset Save...

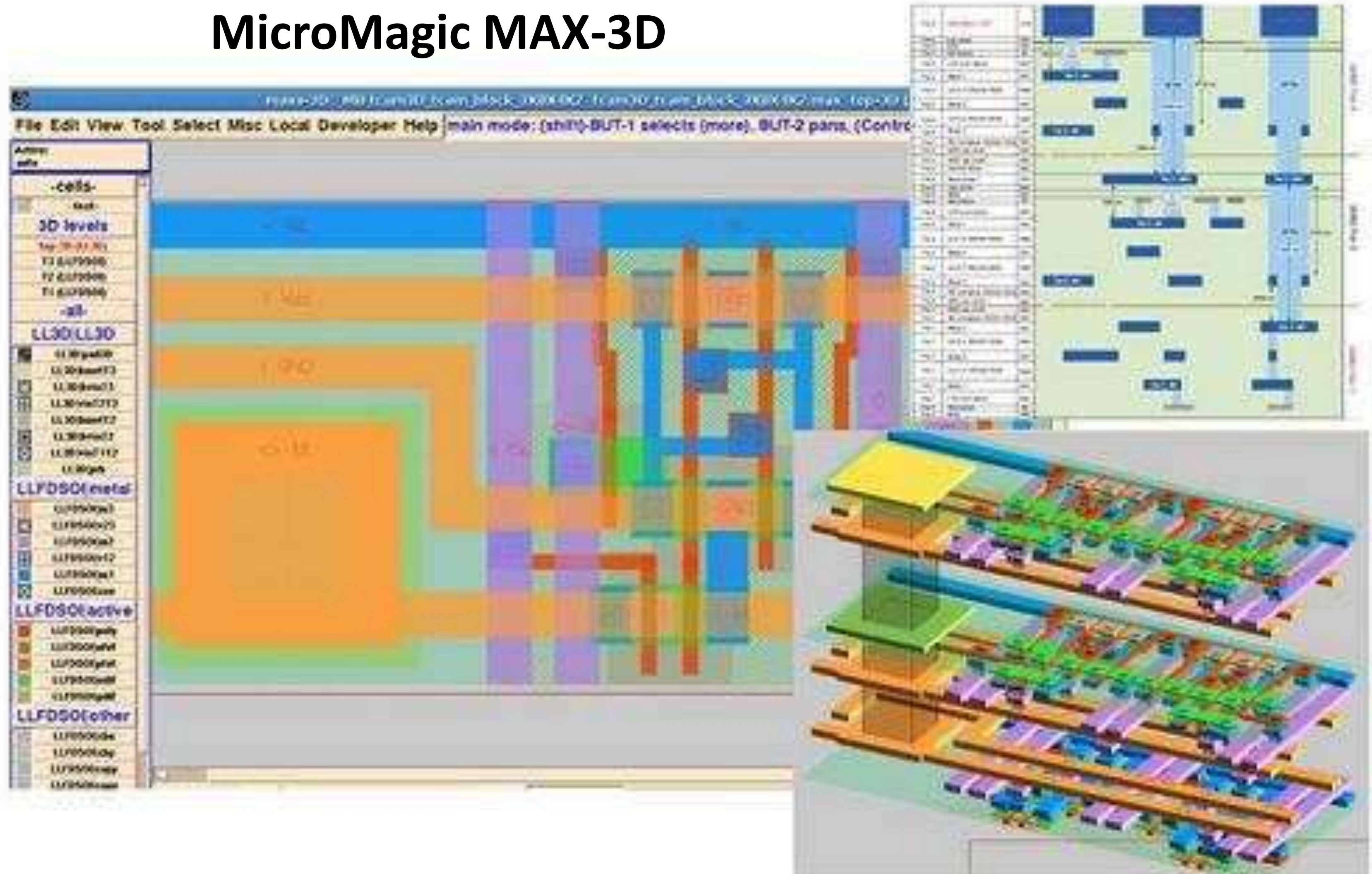
Virtuoso / Calibre LVS Interactive Menu

Choosing 2D or 3D LVS

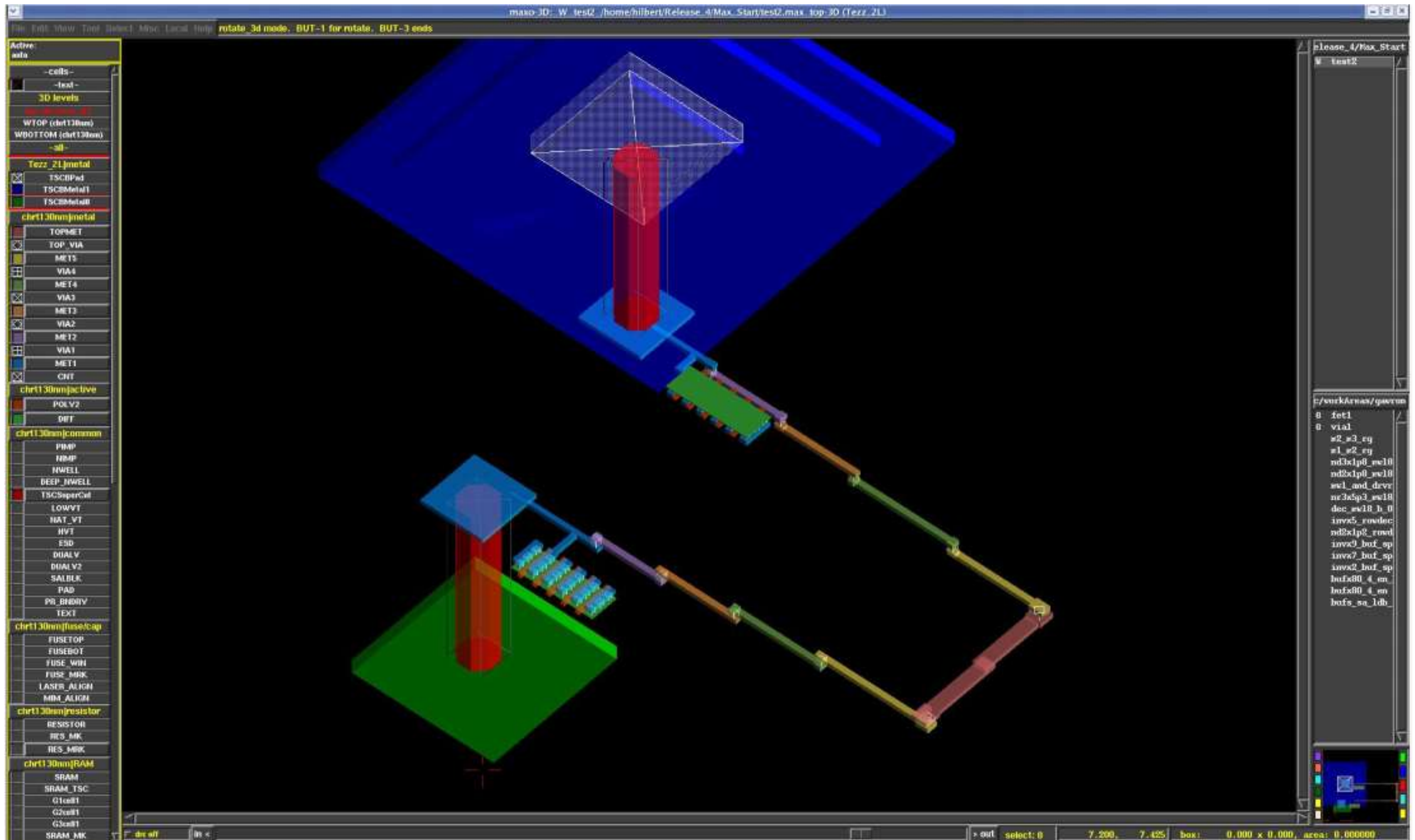
True 3D Mask Layout Editor

Technology Files fully supported by Tezzaron

MicroMagic MAX-3D

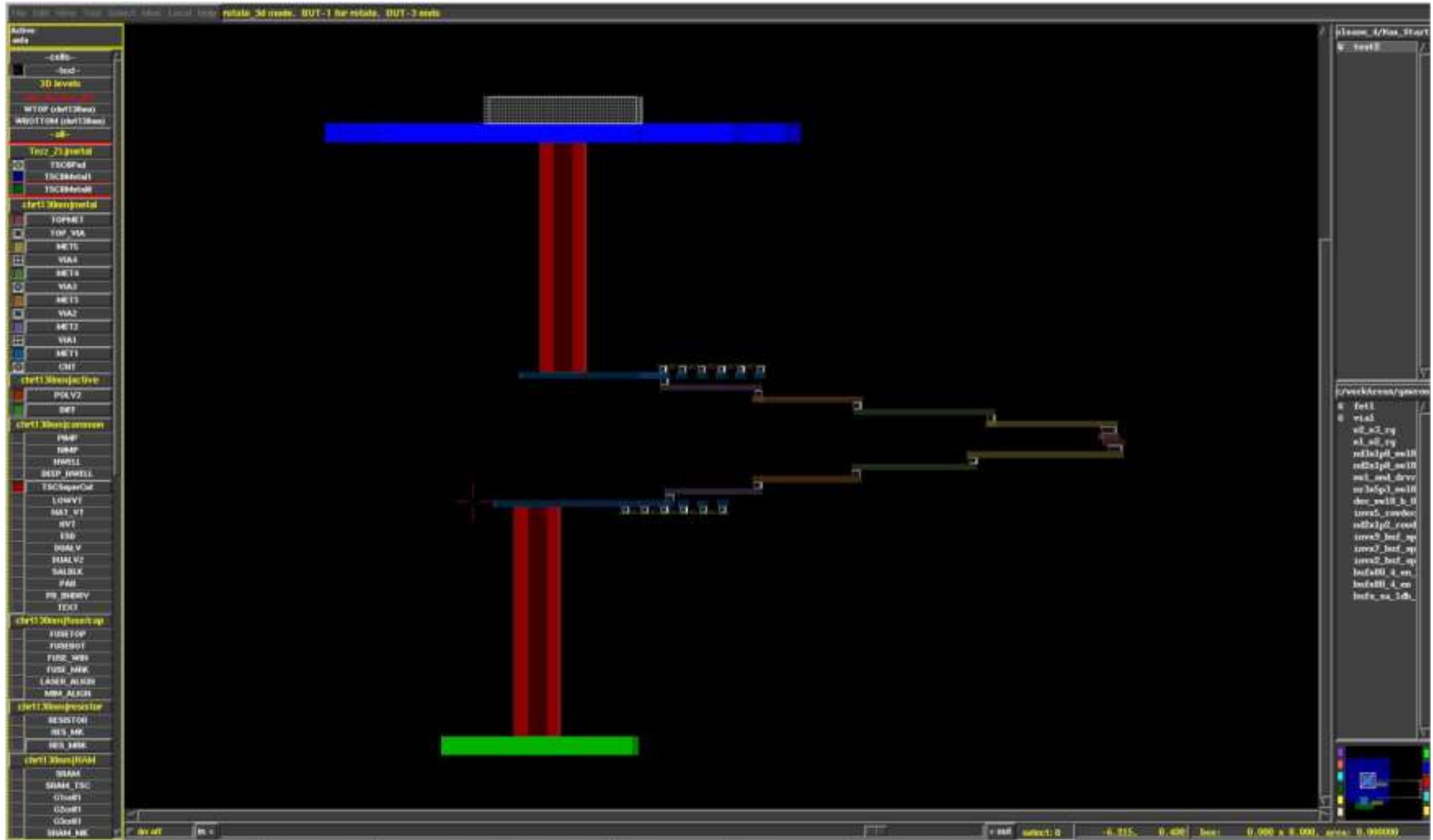


MicroMagic 3D viewer



MicroMagic 3D crossection

CNRS – INPG – UJF

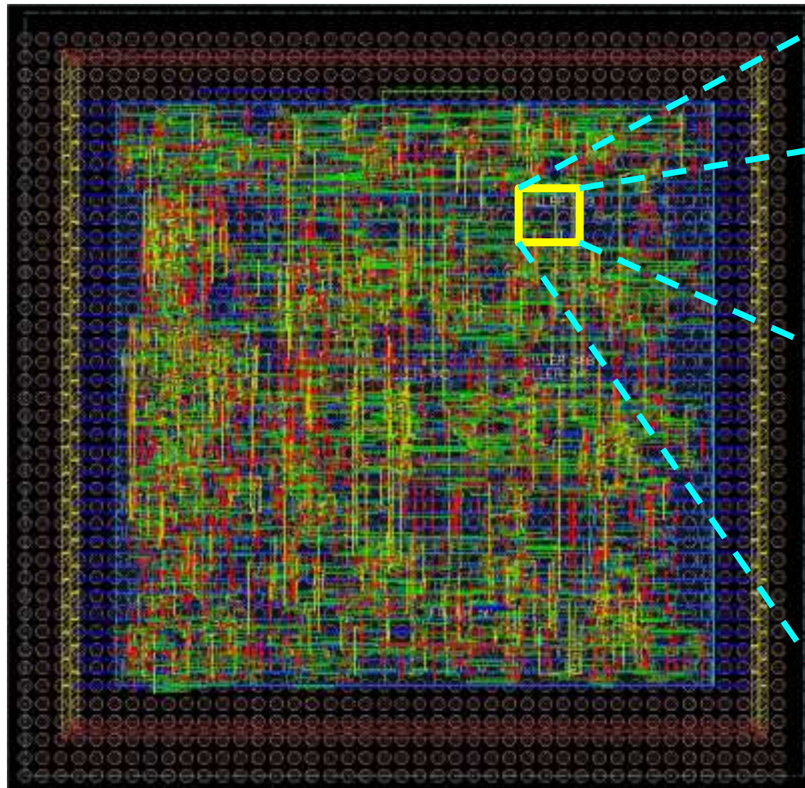


3D-IC Automatic P&R using DBI and TSV

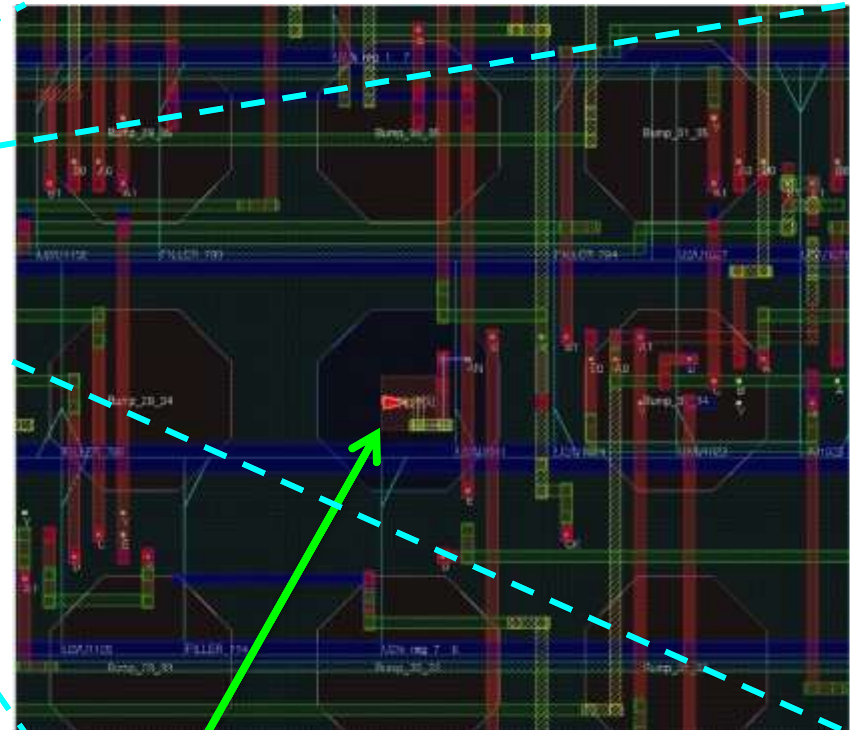
Step	Description
System Level Partitioning	Design exploration at system level
3D Floor-Planning DBI, TSV, IO placement	Design exploration at the physical level DBI, TSV, and IO placement & optimization
Automatic Place & Route	Cells and blocks place & route can be done tier by tier
Extraction, Timing Analysis	To be done for each tier, then combined for back-annotation to the 3D top level system
Physical verification 3D DRC, 3D LVS	Similar to the full-custom design flow
Dummies Filling	Similar to the full-custom design flow
Final 3D DRC	Similar to the full-custom design flow

Automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solved the problem. It's a workaround.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc …



DBI array generation + P&R

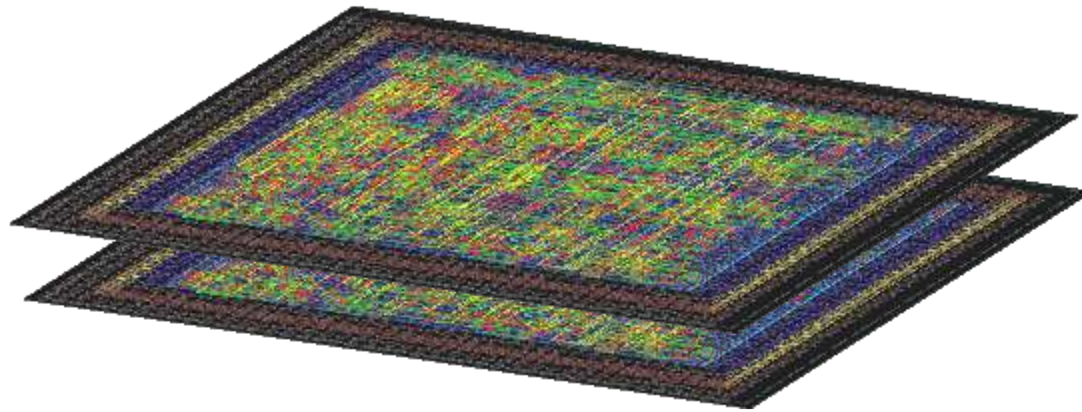


DBI completely routed down to the lower metal layers

Automatic P&R with Direct Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.



This should result in a "correct by construction" design.

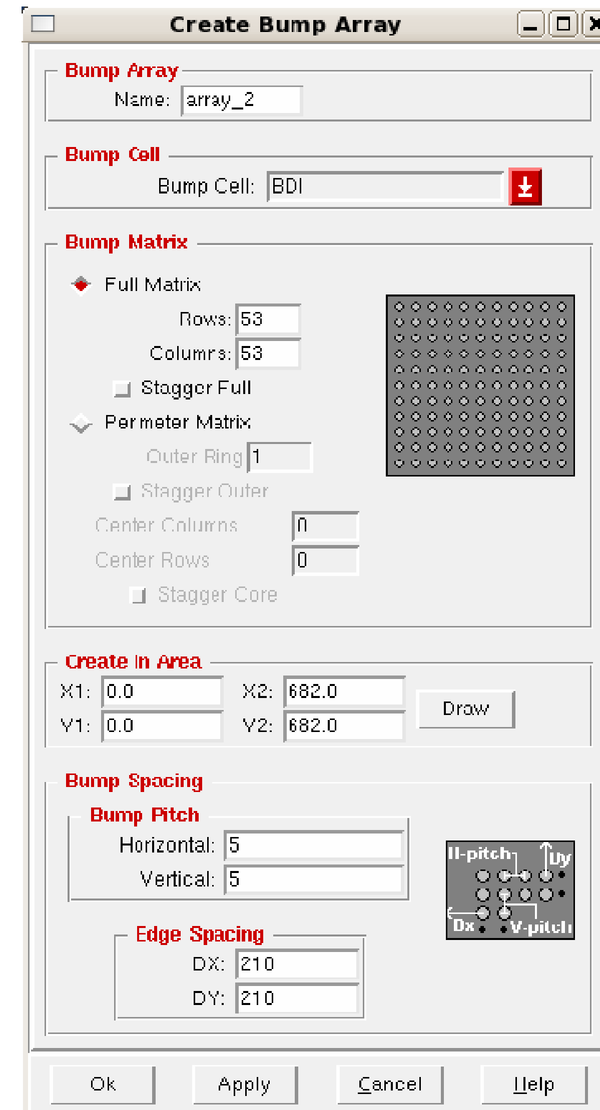
Cadence / Encounter v 8.1 Bump Array Generator

- Create Bump Array

Floorplan > Flip Chip > Create bump Array…

Specify the array Name, number of bumps, pitch, …
Then click OK.

To save an IO file with this bump array choose the following menu:
Design > Save > I/O File…



Cadence / Encounter v 8.1 Signal Bumps Assignment

Floorplan > Flip Chip > Assign Signal…

1. Select the IO signal in the list
2. Select the bump to be assigned
3. Click "Assign". The selected bump become blue.

Assign/Unassign Signals

Signal List

IO Signal	Driver	Cell	Pin	Location	Tile/Bump	Tile Pin	Loc
Filter_In[2]	io_In2	PIC	P	x=0.0 y=411.0			
Filter_In[1]	io_In1	PIC	P	x=0.0 y=341.0			
Filter_In[0]	io_In0	PIC	P	x=0.0 y=271.0			
CLK	io_In_CLK	PIC	P	x=218.5 y=0.0			
RESET	io_In_RESET	PIC	P	x=306.0 y=0.0			
ADC_Busy	io_In_ADC_busy	PIC	P	x=393.5 y=0.0			
ADC_Convstb	(null)		(null)				
ADC_Rd_csb	(null)		(null)		Bump_22_26		x=318.3
Filter_Out[7]	(null)		(null)		Bump_35_33		x=383.3
Filter_Out[6]	(null)		(null)		Bump_29_33		x=353.3
Filter_Out[5]	(null)		(null)		Bump_23_33		x=323.3
Filter_Out[4]	(null)		(null)		Bump_17_33		x=293.3
Filter_Out[3]	(null)		(null)		Bump_35_19		x=383.3
Filter_Out[2]	(null)		(null)		Bump_29_19		x=353.3
Filter_Out[1]	(null)		(null)		Bump_23_19		x=323.3
Filter_Out[0]	(null)		(null)		Bump_17_19		x=293.3

Number of Io Signals: 21

Assign to Tiles/Bumps
- In Select Set
- In Created Order
- Closest

Set Order: As Is

Set Net Wire Width
Wire Width: [ ] Set

Assign | Unassign | Done | He

Encounter® Digital Implementation System RTL-to-GDSII 8.1 - /cmp/ho

Design Edit Synthesis Partition Floorplan Power Place Clock Route Timing SI Verify Too

All Colors

V S

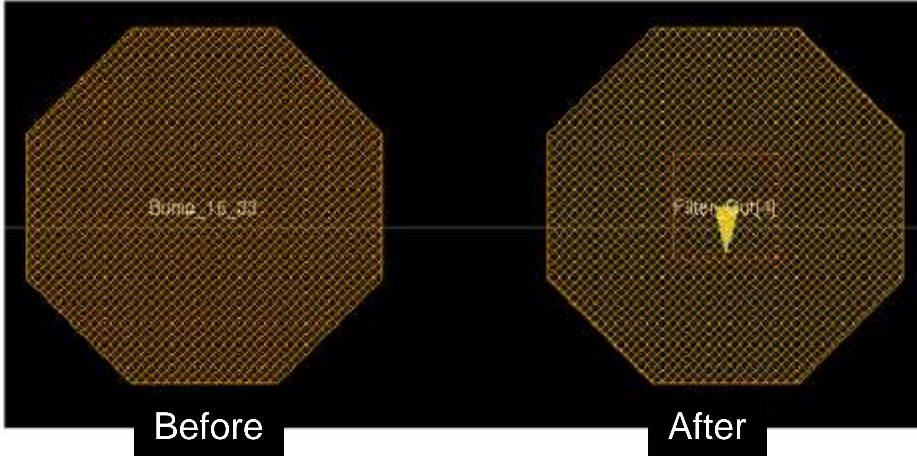
FPlan View, Module, Fence, Guide, Obstruct, Region, Area Density, Instance, Std. Cell, Cover Cell, Block, IO Cell, Area IO Cell, Net, Special Net, Terminal, Ruler, Text, Rel. FPlan, Yield Cell, Yield Map, SDP Connect, Density Map

1 (332.952 , 273.339)

Custom Scripts Enabling Routing on DBIs

Create pins under bumps:

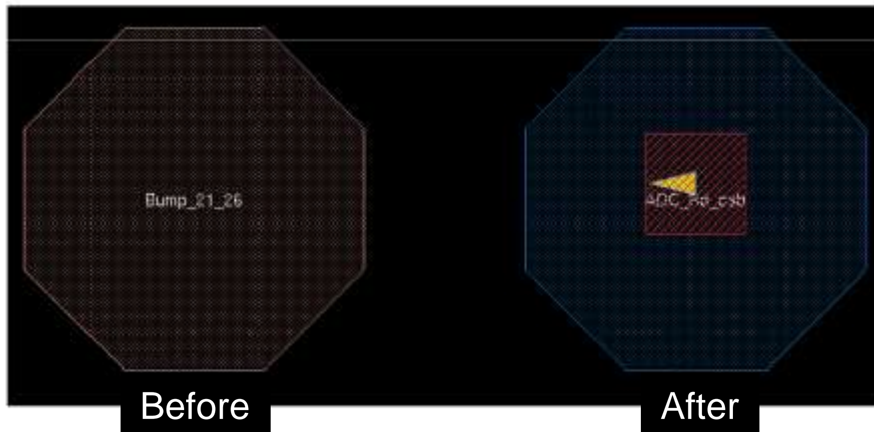
```
exec ../ScriptsBDI/makePhysical_Pins.sed Design_pins_bumps.io makePhyPins.do
```



Placing logical pins on bumps (DBIs), and extract their location.

Generating physical pins under bumps:

```
source makePhyPins.do
setBumpFixed –allBumps
```



Generating Physical pins from these locations.
They can now be used as terminals for routing.

Automatic P & R Design Flow (From Floor-Plan to Routed Design)

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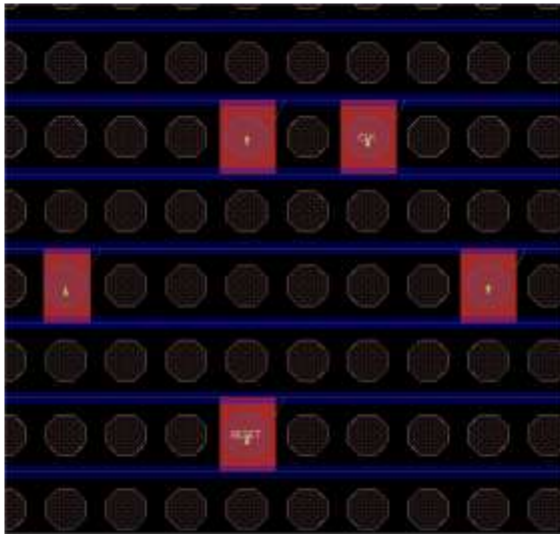
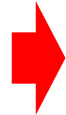
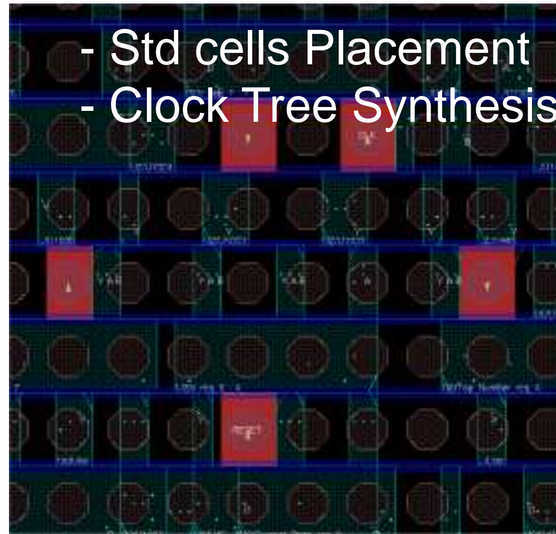
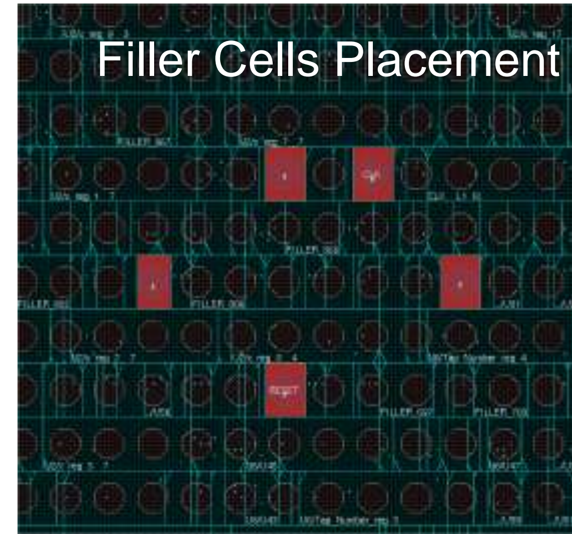


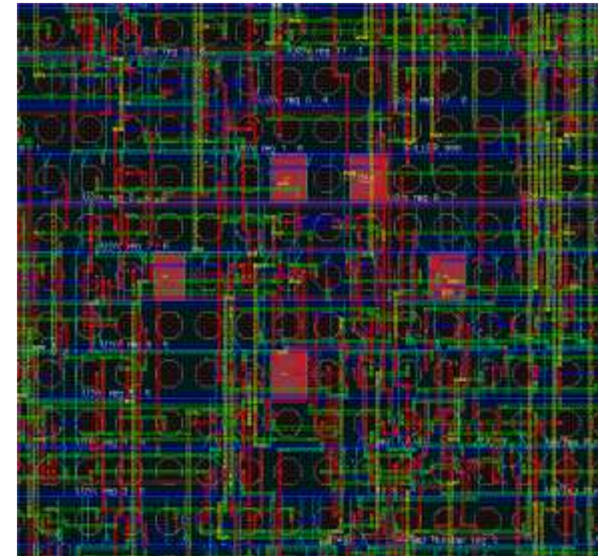






- DBIs Placement
- TSVs Placement
- Obstructions on TSVs

- Clock routing
- Final routing



Clock and all nets routing is enabled on M1-M5

⚠ **The M6 layer must not be used during routing. This layer is reserved for DBI.**

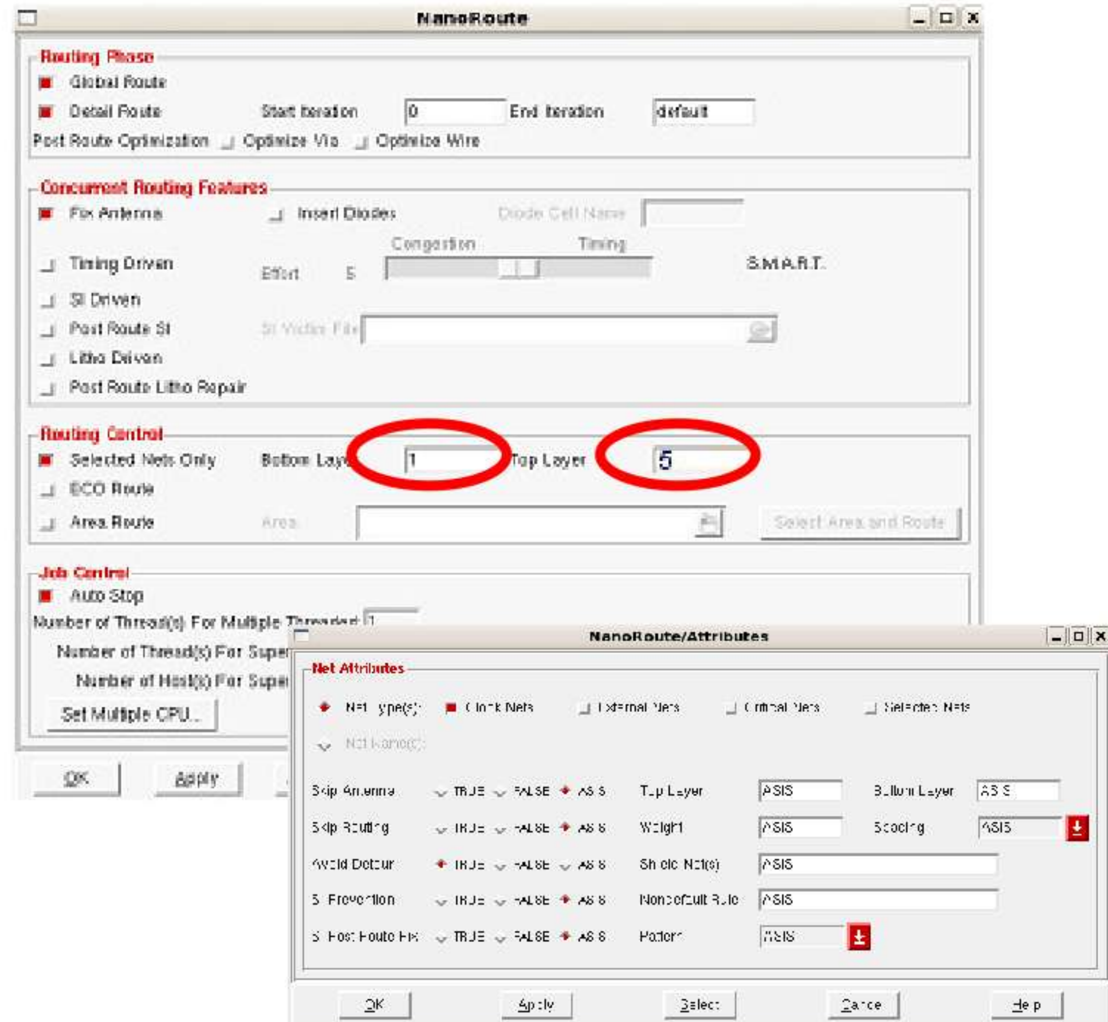
➢ Routing Clock Nets

Route > NanoRoute > Route…

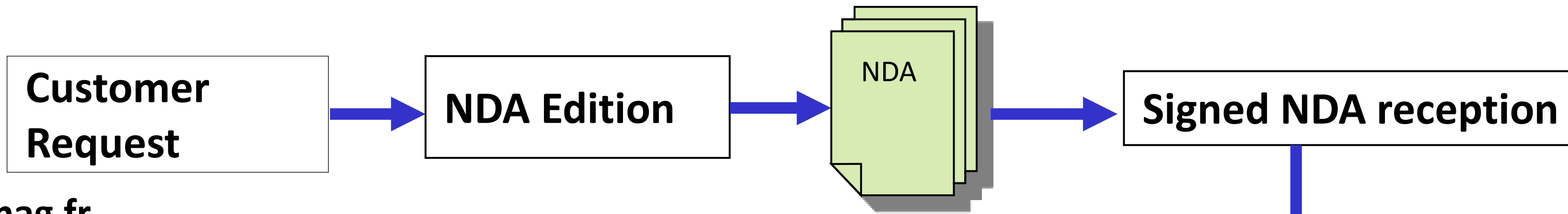
Switch **Selected Nets Only** in the *Routing Control* panel.

In the **Attribute** Menu, select :
Net Type : **Clock Nets**
Avoid Detour: **True**
(this allows to route the clock nets as straight as possible)

Use the "Mode setup" panel to switch the different options (for example, define the bottom/top routing layer).
Click OK to run Nanoroute.



Access to the Design-Rules and the Design Platform



http://cmp.imag.fr

Request to access from CMP Web page or by E-mail to :

cmp@imag.fr

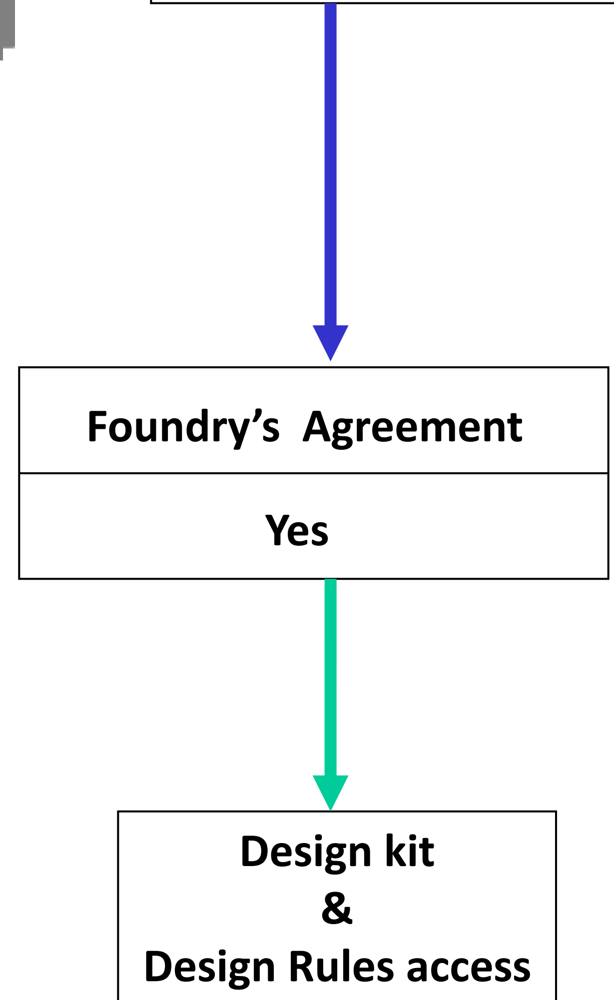
The user receive by E-mail the NDA + ARM lirary Addendum.

The user sign and return by post 2 original signed copies

CMP forward to Tezzaron the NDAs.

When Tezzaron is OK, they counter-sign and return one copy to CMP.

CMP return the copy to the user and give the access to the DRM and Design-Platform.



Users having access to the Design Platform

CPPM, Marseille
IPHC, Strasbourg
LAL, Orsay
LPNHE, Paris
IRFU, CEA Saclay
LAPP, Annecy-Le-Vieux *
ENSTA PARISTECH, Paris *
ISEA, Toulouse

France

INFN, Roma
INFN, Pavia
INFN, Pisa
University of Bologna *
University of Perugia

Italy

University of Bonn, Germany

University of Barcelona, Spain
IMSE-CNM-CSIC, Sevilla, Spain

University of Turku, Finland

Acreo AB, Norrköping, Sweden

Norwegian University, Trondheim, Norway

New Users

Tezzaron Semiconductor, USA

FermiLab, USA

North Carolina State University, USA

MOSIS, USA
CMC Microsystems, Canada

University of Sherbrooke, Canada

+ Other centers supported by MOSIS and CMC
Not listed here.

More than 19 Users in Europe

CNRS – INPG – UJF

Conclusion

- A very collaborative work has been achieved and still ongoing between the parties CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU.

A Design Platform resulted from the collaboration.

(Industrial CAD vendors just starting addressing the features)

- First MPW run deadline : May 31st, 2011

- The community is awaiting for new CAD tools dedicated to 3D-IC Integration :

  + 3D-IC Partitioning : both at the system level and the floor-planning level.

  + Sign-off tools for 3D-IC Integration : (3D-DRC, 3D-LVS, 3D-Extration)